

DESIGN OF SIGE BICMOS RF BUILDING BLOCKS FOR EXTREME-ENVIRONMENT APPLICATIONS

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by

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SUMMARY

The objective of this research is to understand the behavior of RF circuits for extreme-environment applications under intense-radiation and cryogenic operation. In order to mitigate the impact of single-event effects (SEEs), mitigation techniques using silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technology have been investigated. In this work, SiGe HBT-based RF circuits including switches, low-noise amplifiers, mixers, and receivers are designed for SEE mitigation by various radiation-hardening-by-design approach. In addition, the impact of technology scaling on hardening approach as well as cryogenic operation of inverse-mode SiGe HBT LNA will be addressed. Design of high-performance RF building blocks including a power divider/combiner and an attenuator has been discussed.

1. Optimization of SEE-mitigated SiGe-HBT RF switches. This work has been published in IEEE Transactions on Nuclear Science (TNS) © 2015 [64].
2. Design of radiation-hardened RF LNAs. This work has been published in IEEE Transactions on Nuclear Science (TNS) © 2014 [23].
3. Investigation of the use of inverse-mode SiGe HBTs in mixers. This work has been published in IEEE Transactions on Nuclear Science (TNS) © 2016 [65].
4. Design of RF receivers for SEE mitigation in SiGe BiCMOS platform.
5. Cryogenic characterization of radiation-hardened LNAs.
6. Design of wideband, low-loss, digital-step attenuators.
7. Design of a wideband, bi-directional, active power divider/combiner circuit
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CHAPTER 1. INTRODUCTION

1.1 Motivation

Operation of electronics in extreme environments typically imposes severe constraints on the constituent circuits and systems. They should provide stable performance under the radiation effects and wide/extreme temperature range. In addition, performance-driven design is often necessary due to the tough requirements such as high speed, large bandwidth, and high resolution. With regard to extreme environment electronics, silicon-germanium (SiGe) heterojunction bipolar transistors (HBT) are well known for their tolerance against total ionizing dose (TID) up to multi-Mrad and inherent high speed and large bandwidth [1]-[3]. This is a significant benefit over the conventional CMOS devices, where the dielectric oxide layers are much more vulnerable to long-term damage from total dose exposure. However, SiGe HBTs are known to be sensitive to single-event effects (SEE), which produce abrupt current and voltage spikes when a high energy particle strikes the active region of the device [1]. These single-event transients (SETs) often lead to distorted output waveforms in analog applications [4], [5].

When it comes to the radiation effects in radio frequency (RF) SiGe circuits, most of the previous studies have limited to their focus to the forward-mode (FM) operation due to the inevitable performance degradation associated with the inverse-mode (IM) operation [4], [6]. Fortunately, however, with the benefit of SiGe technology scaling, the unity-gain frequency (f_T) and the maximum oscillation frequency (f_{MAX}) of IM SiGe HBTs have been significantly improved, now offering several tens of GHz operational performance [7], [8], suggesting that the IM SiGe HBT can potentially be utilized in space-based RF circuits and

systems. Thus, the IM operation can provide assistance in mitigating SET sensitivity for high-frequency circuits [4], [5]. Throughout this dissertation, the design of SET-hardened RF circuits utilizing IM SiGe HBTs will be presented. In addition, low-temperature (cryogenic) operation will be characterized for SET-hardened RF low-noise amplifiers (LNAs). Lastly, in the perspective of conventional RF circuit design, several designs of high-performance RF building blocks in SiGe BiCMOS platform will be shown for their potential use in extreme environment applications.

1.2 Research Objective

The objective of this research is to design RF circuits optimized for extreme environment operation. Among various phenomena associated with extreme environment conditions, the SETs in RF circuits are investigated and minimized by a radiation-hardening-by-design (RHBD) approach. First, three types of RF circuits will be optimized for SET mitigation: RF single-pole single-throw (SPST) switches, low-noise amplifiers, and down-conversion mixers. For RF switches, a SiGe HBT-based topology is proposed and its configuration is optimized for mitigated SETs. In the LNA study, an IM SiGe HBT is utilized in a cascode core for reducing SETs and minimizing RF performance. For mixers, IM SiGe HBTs are applied for a switching pair, showing potential SET mitigation capability for large-signal operation. With these components, SET-hardened RF receivers will be designed and characterized.

The next topic is to investigate the impact of technology scaling for the application of SET-hardening techniques to RF circuits. After recent trends in RF performance will be summarized over the different technology generations, the application of IM SiGe HBTs

will be analyzed for SET mitigation with acceptable RF performance. Specifically, the IM SiGe HBTs will be utilized for active gain stages in RF LNAs. In addition, the operation of RF LNAs in cryogenic conditions will be studied for wider applicability of the IM SiGe HBTs in extreme environment electronics.

In terms of conventional RF circuit design, the last section of this dissertation will focus on the design of RF building blocks for RF system applications. Since many extreme-environment electronic systems require high-performance component circuits, we will demonstrate key building blocks for wideband radars and transceivers. The design of a wideband bi-directional power divider/combiner and an attenuator in SiGe BiCMOS technology platforms will be discussed.

1.3 Literature Survey

It is well known that silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) are inherently tolerant to total ionizing dose (TID) radiation compared to their conventional CMOS counterparts, where dielectric oxide layers are much more prone to long-term TID damage [1], [9]. Furthermore, with their favorable high frequency figure-of-merits such as unity-gain frequency (f_T) and maximum oscillation frequency (f_{MAX}), SiGe HBT technologies exhibit strong potential for RF/millimeter-wave applications under extreme environment conditions [10], [11]. In spite of these advantages, SiGe HBTs still suffer from SEE, which causes abrupt voltage and/or current spikes at device terminals when high energy heavy ions strike the junction area of the active devices. These single-event transients (SETs) may lead to distortions in signals, and thus, they are detrimental to signal integrity, possibly resulting in loss of data [12]-[14]. In addition, high peak voltages

or currents can degrade device reliability, leading to leakage increases, performance degradation, or even device failure [15], [16].

With regard to SET-mitigated RF circuits, there have been a number of studies in the literature investigating SETs and their mitigation in SiGe HBT-based RF circuits [17], [18]. While most of the previous research has to date been mainly limited to active circuits such as amplifiers and oscillators, where SiGe HBTs are biased in a forward-active region in order to achieve large gain or transconductance (g_m), little has been addressed for the operation of SiGe HBTs in their saturation region. Since the saturation region can have unique applications in RF switching circuits, it is important to characterize and understand the impact of using saturated SiGe HBTs in RF switches in terms of SET peak and duration as well as RF performance. Regarding the design of SET-hardened RF low-noise amplifiers (LNAs), the use of inverse-mode (IM) SiGe HBTs is focused on for SET mitigation in this dissertation. Recently, the IM SiGe HBT, in which the physical emitter and collector terminals of the device are swapped, has been suggested as a RHBD approach [19], [20]. This IM RHBD technique has been applied to logic circuits and, as a result, the single-event upset (SEU) sensitivity was reduced compared with conventional forward-mode (FM) designs [19], [20]. The study of radiation effects in RF SiGe circuits has to date been limited to FM operation due to the inevitable performance degradation that results from IM operation [4], [6]. When it comes to RF down-conversion mixers, the IM SiGe HBTs were also utilized for SET mitigation. In the literature, the applicability of IM SiGe HBTs to analog design, to date, has been limited to DC or small-signal circuits [21], [22], [23].

Aggressive scaling down of a SiGe HBT technology has significantly improved the RF performance of IM SiGe HBTs (as well as FM ones), extending the peak f_T of IM SiGe

HBTs beyond several tens of GHz [24]. This implies that the IM SiGe HBTs can potentially be utilized as active gain stages for space-relevant low-GHz RF circuits without substantial performance loss. In this dissertation, an RF (2.4 GHz) LNA is selected to characterize the impact of IM SiGe HBTs on RF circuit performance and investigate the achievable SET mitigation as a viable radiation-hardening-by-design (RHBD) approach. While the IM SiGe HBTs have shown a mitigated transient response, it is necessary to characterize the cryogenic operations of IM-based RF circuits in order to verify their potential use for extreme-environment applications. However, most studies in the literature have focused on the cryogenic operations of the forward-mode-based SiGe HBT circuits [25]-[29].

The design of high performance RF circuits including a power divider/combiner and an attenuator will be discussed. There have been a number of approaches for designing power dividers and combiners in the literature. One of the conventional designs is a passive-type power divider (or a combiner) such as the Wilkinson divider [30]. However, they have the disadvantages of insertion loss, limited bandwidth, and large size. As an alternative, active-type power dividers and combiners, which use active gain stages for signal amplification, have been suggested as an alternative approach for passive-type circuits [31]-[38]. However, they still exhibit limitations of unidirectional operation, integration with digital circuitry, and narrow bandwidth. With regard to the attenuator design, attenuators are used in the control of side-lobes in antenna radiation patterns [39]. Recent state-of-the-art digital-step attenuators (DSAs) have utilized T- or π -type attenuation cells and series/shunt switches for path selection control [39]-[41]. However, the previous studies show high insertion loss associated with each series switch transistor [39] and large chip size due to many inductors for internal/external matching [41].

CHAPTER 2. DESIGN OF SEE-HARDENED RF CIRCUITS

2.1 Optimization of SiGe-HBT RF Switches for SEE Mitigation

2.1.1 Introduction

SPST RF switches are key components for implementing various types of RF communications systems, including ultra-wide-band (UWB) impulse radio, on-off-keying (OOK), RF power-protection circuitry, etc. For example, a UWB impulse radio transmitter is shown in Figure 2.1.1 [42]. In this system, signals typically propagate in one direction and the high reverse isolation strongly suppresses the backward signal. Hence, an SET occurring at the SPST switch can have a critical impact on the operation of the subsequent blocks by changing bias conditions or saturating the power handling capability.

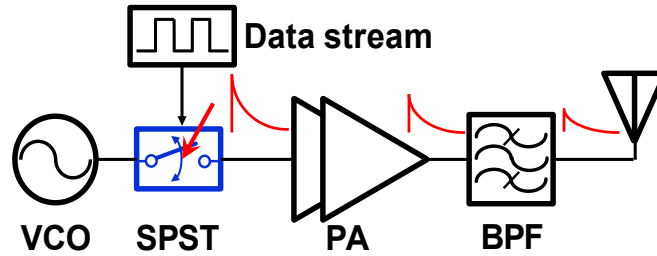


Figure 2.1.1 - Simplified transmitter architecture for ultra-wideband impulse radio applications.

The conventional SPST switch employs two transistors: one in series, and the other in shunt [43]. The resistors at gate and body terminals are used to prevent leakage of the RF signal [44]. Since in the case of SiGe HBTs the emitter and the collector terminals are asymmetric, we can think of four different types of SPST cores based on the terminal swapping for series and shunt devices, as shown in Figures 2.1.2 (a) - (d). When the

physical emitter of a SiGe HBT is used as an output terminal, the transient peak and duration are generally reduced when compared with the collector connected to the output terminal [23]. This is because the emitter has higher isolation against the ion-induced subcollector-substrate tail current reaching the electrical collector (i.e., the SPST output) [19], [20].

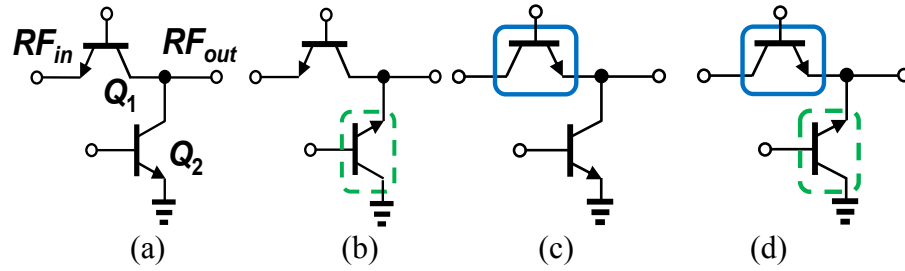


Figure 2.1.2 - SiGe HBT switch cores: (a) (forward) connection for both series and shunt devices (F-F), (b) forward connection for series device and reverse connection for shunt one (F-R), (c) R-F, and (d) R-R.

2.1.2 TCAD SET Simulations

To compare and optimize SET mitigation capabilities, a two dimensional (2-D) TCAD model for an IBM 8HP 130 nm SiGe HBT [45] was developed and implemented in Sentaurus tools. The model was calibrated against DC and AC data using measured the Gummel and f_T characteristics of a 120 nm x 2.5 μm device. Figure 2.1.3 shows the vertical structure of the TCAD model. The SiGe HBT was isolated by a deep-trench (DT) placed around the active device region and the device terminal layout was configured as collector-base-emitter-base-collector (CBEBBC) for better RF performance by minimizing parasitic resistance associated with the base terminals [46]. For heavy-ion simulations, the direction of ion strike is perpendicular to the emitter-base (EB) and collection-base (CB) junctions

(orthogonal to the surface) to maximize electron-hole pair generation. This represents a worst case strike condition.

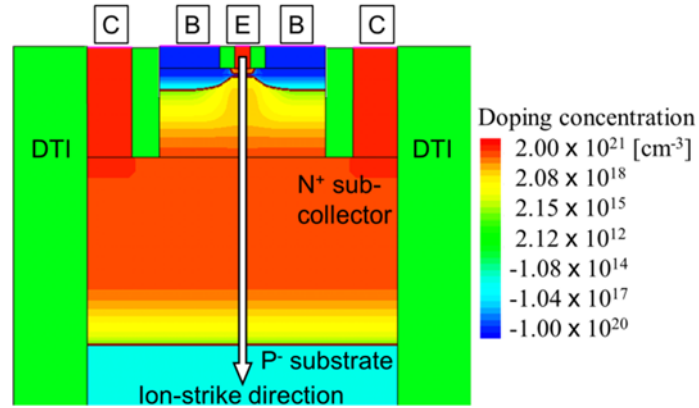


Figure 2.1.3 – Two-dimensional device structure of a single SiGe HBT for TCAD simulation.

The transient simulation results under a heavy-ion strike are shown in Figure 2.1.4 (a) and (b). The value of linear energy transfer (LET) used in the simulation was $1.94 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. In series device strike cases (Fig. 3 (b)), the reverse-connected series SiGe HBTs (R-F and R-R in Figure 2.1.2) exhibit smaller transient peaks and shorter durations. This is because the emitter terminal is better isolated from the substrate-subcollector junction than the collector terminal, thereby reducing the current spike at the emitter [8]. Furthermore, this isolation will contribute to a shorter transient duration at the emitter terminal, since the larger portion of the substrate-subcollector tail current will flow out of the collector terminal. Hence, it is reasonable for RF SPSTs to use reverse-connected series SiGe HBTs in order to minimize the impact of heavy-ion strike on the series device to the subsequent RF chain (Figure 2.1.1).

Similarly, for shunt device strike cases (Figure 2.1.4 (b)), the reverse-connected configurations (F-R and R-R in Figure 2.1.2) are suitable from an SET reduction

perspective in terms of both peaks and durations. However, the overall response shape of forward-connected and reverse-connected cases are different, in that the reverse-connected shunt SiGe HBTs show peaks about 0.5 ns later than the ion-spike time, whereas the forward-connection cases have almost immediate transient peaks. From these simulations, we can conclude that the R-R core is well-suited for SET-hardened RF SPST design, and the laser-induced beam experiment results confirming this will be shown in the next section.

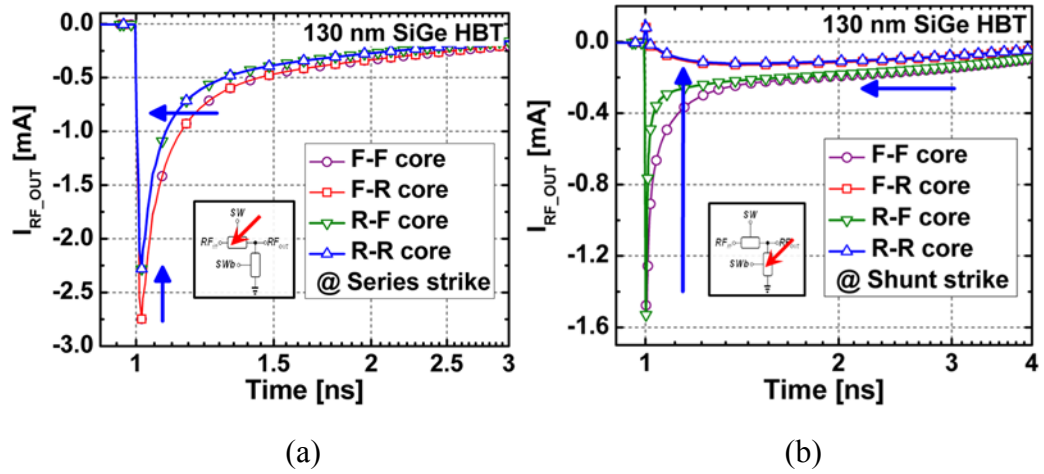


Figure 2.1.3 - Heavy-ion simulation results of (a) series device strike and (b) shunt device strike for different RF switch configurations.

2.1.3 Pulsed-Laser Experiment Results

To characterize and verify the SETs within the switch cores, the laser-induced beam experiment was conducted at the U.S. Naval Research Laboratory (NRL) using a through-wafer, two-photon absorption (TPA) pulsed-laser single event effect technique (PLSEE) [47], [48]. The laser-induced beam has 150 fs pulse duration at a wavelength of 1.26 μm and 1.2 μm full width half maximum (FWHM) spot size. In order to fully capture the

transient signals at the DUT terminals, a high speed oscilloscope (Tektronix DPO71254) and specially-designed test boards were used.

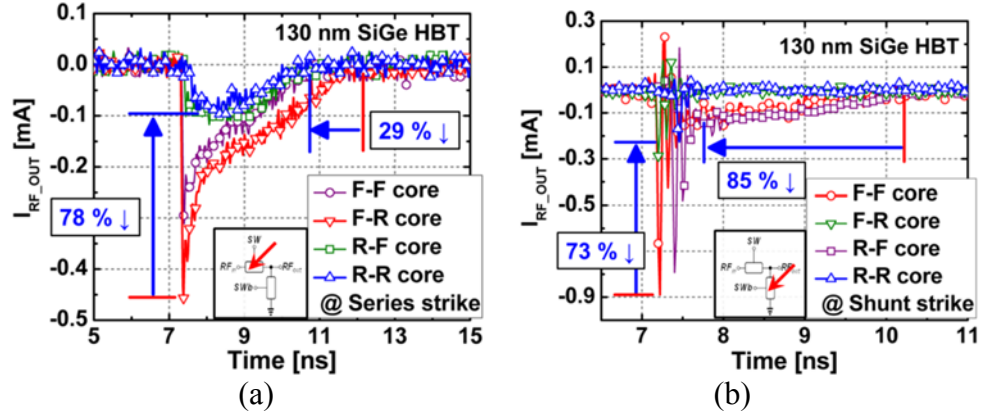


Figure 2.1.4 - Time domain responses of SETs for different series-shunt configuration under (a) series strike and (b) shunt strike. The R-R configuration has the minimum peaks and durations in both strike cases.

In Figure 2.1.4, the time domain responses of the SETs for both series and shunt strike cases from four different switch cores are compared. For the best switch performance, the base terminal voltage of the series devices was about 0.85 V, and both the emitter and the collector terminals were connected to ground by bias tees. In the series strike (Figure 2.1.4 (a)), the forward connection of the series devices (F-F and F-R) has higher peaks than those of the reverse connection (R-F and R-R), as expected from the simulation results. Another observation was that the time when the transient peaks occur for reverse series devices was about 0.7 ns later than for forward connection cases. The delayed peaks in the reverse series devices can be attributed to their large output resistance at the physical emitter nodes, thereby increasing time constants. The reverse connection provides higher resistance since the grading of Germanium doping profile in the base region will enhance the internal electric field as opposed to current flow from emitter to collector [49]-[51]. Although the transient peaks occurred later in the reverse series devices

(R-F and R-R), the transient durations were shorter than those of the forward series devices (F-F and F-R). The best and the worst SET responses were the R-R and the F-R core configurations, respectively. The R-R core shows 78% smaller peak transients and 29% shorter duration transients compared to the F-R case.

Figure 2.1.4 (b) shows the similar results under the shunt device strike condition. In this case, the worst SET response was observed for the F-F core, and the best configuration was the R-R core, the same result as in the series strike results. The R-R configuration had a 73% smaller peak and an 85% shorter duration compared to the F-F core counterpart. Thus, these measured SET responses qualitatively validate the relative peaks and durations obtained from the TCAD simulation results (Figure 2.1.3) for the different core configurations.

Compared with the simulation results in Figure 2.1.3 (a) and (b), there are, however, some discrepancies between the TCAD simulations and the experiment data. These mainly originate from: 1) device model calibration issues, 2) parasitic components not included in the modeling, and 3) different simulation set-up conditions. First, since the TCAD model was calibrated with DC and small-signal AC parameters (f_T), the accurate large-signal behavior of SiGe HBTs may not be fully captured in the simulations. In addition, the 2-D model used in the TCAD cannot fully show 3-dimensional physical effects. Second, in the actual experiment, there are many parasitic components associated with wire-bonding, test board, cables, and instruments. These parasitics can potentially modulate the impedances seen at each terminal, thereby changing the SET responses of RF switch cores. Lastly, while in the TCAD simulation the heavy ion passes vertically through the substrate, the laser-induced beam needed to focus two photons to a certain point in a vertical axis. Thus,

the number of carriers generated during the experiments and their trace can be different from the heavy-ion simulation set-up. However, the overall qualitative trends in SET peaks and durations match with the TPA pulsed-laser experiment results, thereby enabling meaningful optimization of the RF SPST designs.

The time domain waveform can be Fourier-transformed in order to analyze the data in the frequency domain. This gives additional information which is often very useful to high frequency circuit and system designers. For example, additional filters should be inserted at the output of RF SPST to minimize the impact of SETs to subsequent circuits. The type of filters can be low-pass, high-pass, or band-pass depending on the actual frequency corruption that the heavy-ion strike produces.

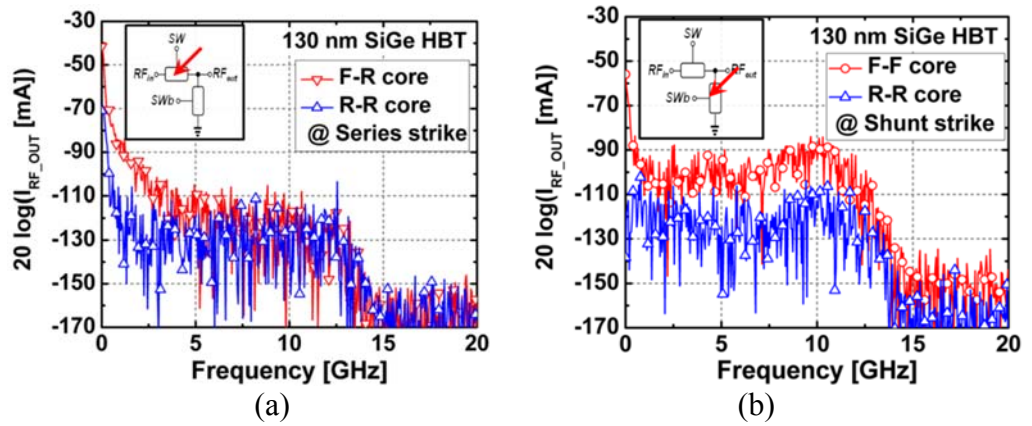


Figure 2.1.5 - Frequency spectrum of SETs under (a) series strike and (b) shunt strike. Only the best and the worst cases are compared. The R-R configuration has the minimum peaks and durations in both strike cases.

The frequency spectra of both the series and shunt strike cases are shown in Figure 2.1.5. These data were obtained by applying a fast Fourier transform function (FFT) to the data in Figure 2.1.4. In Figure 2.1.5 (a), the F-R core has larger (worse) low frequency content up to 6 GHz. The maximum difference between the F-R core and the R-R core was

about 30 dB. Above this frequency, the spectral differences become negligible. Since the high frequency region (> 15 GHz) is out of the measurement bandwidth, the data in that range may come from the instrumental noise or quantization errors. Figure 2.1.5 (b) shows the frequency spectra of the shunt device strike. Note that there is a local maximum near 10 GHz. This can be inferred from Figure 2.1.4 (b), since it shows short-period ringing response at the beginning of the strike. In addition, the R-R core has no apparent peak at the DC points; meaning, the overall DC fluctuation was not dominant.

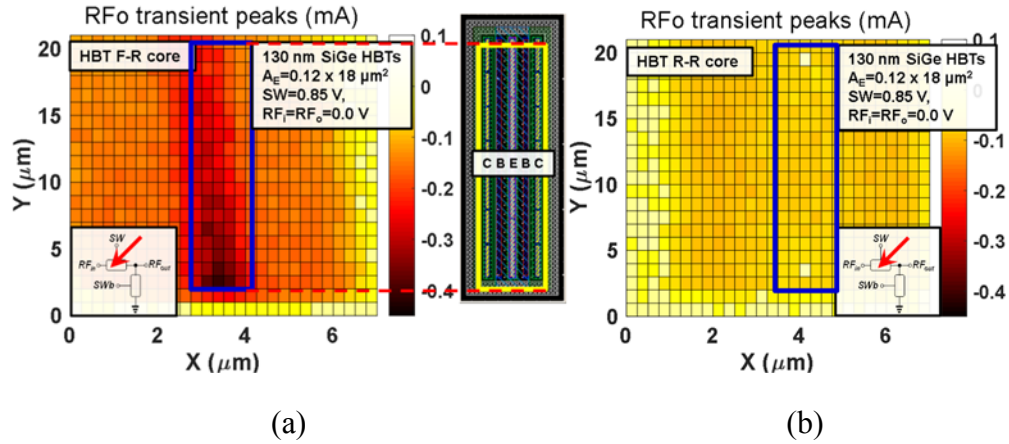


Figure 2.1.6 - Two-dimensional raster scans of series device strike for (a) F-R and (b) R-R configurations. Only the best and the worst cases are shown. The transistor layout of the same size is shown in the middle. The HBT has collector-base-emitter-base-collector (CBEBC) terminal layout.

The 2-D raster scan of both the series and the shunt strike cases, when the switch cores are ON, are shown in Figure 2.1.6 and Figure 2.1.7, respectively. With the actual transistor layouts, the sensitivity of each strike point can be mapped. Dark red and white points show the highest and the lowest sensitivity under laser-beam exposure, respectively. The R-R core has significantly smaller transient peaks compared to the worst cases (F-R for series strike and F-F for shunt strike), implying that the R-R core is the most suitable SET-hardened configuration from a system level perspective. In addition, when the switch

cores are OFF, with the series device OFF and the shunt device ON, the R-R core still exhibits the minimum SET peaks and durations at the output terminal (data not shown here). Therefore, it is concluded that the R-R core is the best configuration for SET mitigation.

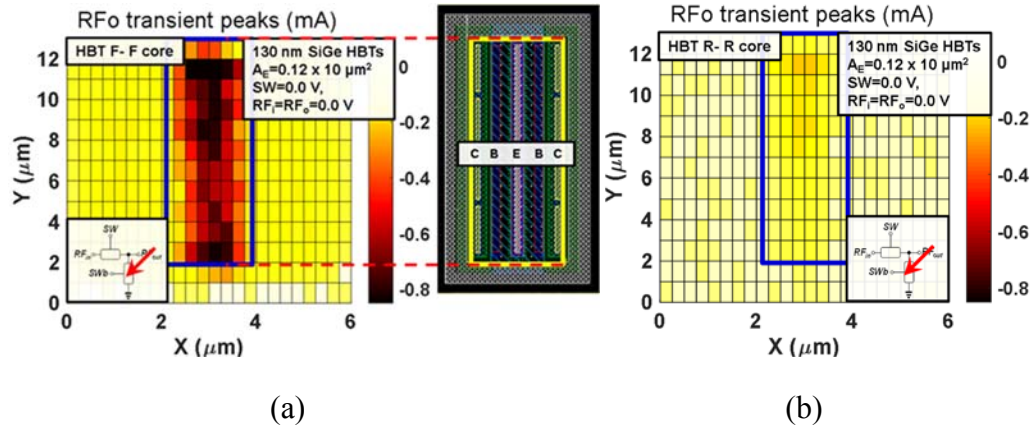


Figure 2.1.7 - 2-D raster scans of shunt device strike for (a) F-F and (b) R-R configurations. Only the best and the worst cases are shown. The transistor layout of the same size is shown in the middle.

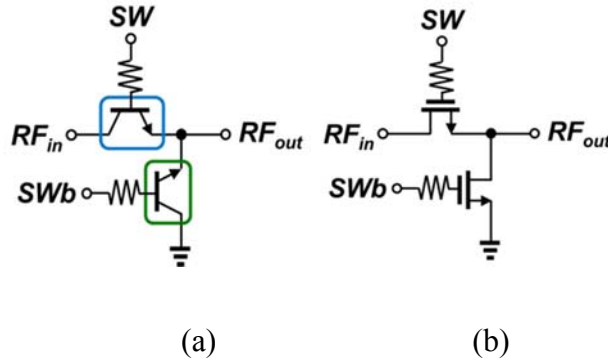


Figure 2.1.8 - Simplified schematic of a fully-integrated SiGe HBT-based SPST (left) and an FET-based SPST (right).

To further investigate the trade-offs of using SiGe HBTs in RF SPST switches, the TPA pulsed-laser beam experiments were also conducted for both fully-integrated FET-based and SiGe HBT-based SPSTs. The simplified schematics are shown in Figure 2.1.8. The FET SPST used RF nMOSFETs with a channel length of 130 nm, and found within

the same IBM 8HP BiCMOS technology platform. Large resistors are inserted between gate (or base) nodes and SW (and SWb) nodes to provide open termination for the RF signals.

Figures 2.1.9 (a) and (b) show SET responses of both FET and SiGe HBT SPSTs from TPA laser-induced beam experiment with the same energy level. Under the series strike condition (Figure 2.1.9 (a)), the SiGe HBT (R-R core) SPST has 76% lower peak transient, but the recovery time (duration) was longer than that of the FET SPST, revealing the subtle trade-off for the SET-minimized design. However, under the shunt strike (Figure 2.1.9 (b)), the SiGe HBT (R-R core) has better response in terms of both peak and duration. With respect to device reliability, FETs are more vulnerable to large SET peaks, since the breakdown voltage of FETs is lower than SiGe HBTs. Hence, it is more likely that the abrupt current or voltage spikes can lead to device failure for FET SPSTs. In addition, the large peaks in the FETs may interrupt the DC biasing conditions or degrade the reliability of subsequent circuit blocks.

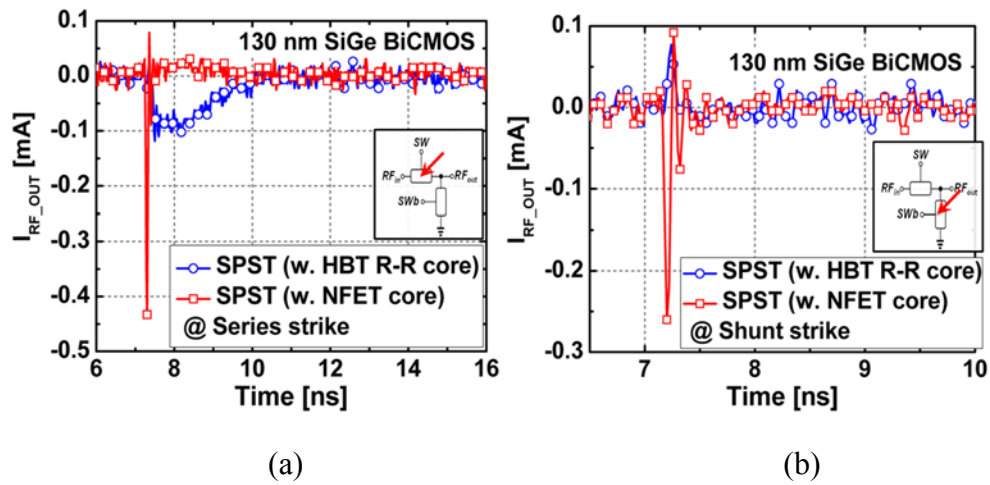


Figure 2.1.9 - (a) SET responses under series device strike. (b) SET responses under shunt device strike. For the series strike, the SiGe HBT SPST with an R-R core exhibits reduced transient peak, but longer transient durations than FET SPST.

2.1.4 Design Consideration and RF Performance Comparison

One of the key differences between designing SiGe HBT SPST switches vs. FET SPST switches is that SiGe HBTs require current-flowing paths to turn ON the device (to bias it in saturation). Thus, there should be two current paths for DC biasing at both emitter and collector nodes for series device. These current paths can be implemented by shunt RF choke inductors or shunt resistors to ground. Since the RF choke inductor has an advantage of maintaining the effective emitter (or collector) DC voltage close to zero due to the negligible resistance associated with spiral metal lines, it is much easier to adjust the base bias voltage or current. However, this requires large chip area and often limits the low-frequency operation. On the other hand, the use of the shunt resistor can simplify SPST switch design and significantly save layout area, while the base to emitter voltage (V_{BE}) or the base to collector voltage (V_{BC}) tuning range become somewhat limited, since the emitter (or collector) node voltage is not fixed and is dependent on the resistance and the amount of current flowing through the resistor.

Besides, the amount of DC biasing current is closely related with RF switch performance. For example, insertion loss (IL) is one of the important parameters for RF switches. In order to reduce IL, the effective on-resistance (R_{ON}) of the series device should be minimized; meaning higher V_{BE} (or V_{BC}) are required for lower IL [52]. However, due to the exponential relationship between V_{BE} and I_C in forward-biased pn junctions, the power consumption of SiGe HBT SPST switches may exceed available system budget. In many cases, the restriction on power budget can limit the achievable IL of SiGe HBT RF SPST switches.

In addition, as mentioned in the previous paragraphs, in SiGe HBT SPST switches, the resistor values should be carefully chosen for the optimal SiGe HBT bias condition, as opposed to FET-based switches, where no DC current flows and resistors can be large enough so that RF signals see the resistors as almost ideal open terminations [44]. In cases where resistors are not very large compared to $50\ \Omega$, RF signal leakage can happen through the resistors, increasing the IL of the SiGe HBT SPST switch. Therefore, these issues should be considered in the design phase of SiGe HBT SPST for optimal RF performance.

Table 2.1.1 – Performance Summary of SiGe-HBT and FET RF Switches

SPST configuration	SiGe HBT (R-R core)	FET (RF nMOS)
bandwidth [GHz] @ corner frequency*	26.4	15.4
bandwidth [GHz] @ 2 dB insertion loss ⁺	36.0	25.0
insertion loss [dB]	1.4	0.8
isolation [dB]	-24.6	-19.5
P1dB [dBm]	13	16
IIP3 [dBm]	24	29
P _{DC} [mW]	0.3	0.0

* Both RF SPSTs operate from DC and the bandwidth is defined as the corner frequency of insertion loss.

+ 2 dB-insertion-loss bandwidth is defined as the frequency when the insertion loss first reaches 2 dB.

The overall switch performance of the SiGe-HBT and FET SPST switches is summarized in Table 2.1.1. Since the RF performance of the four different configurations (F-F, F-R, R-F, and R-R) were similar, only the SPST with the R-R core is shown in Table 2.1.1. The IL of SiGe HBT SPST was 0.6 dB higher than the FET SPST due to the trade-off with power consumption and the limitations on the available resistance for DC biasing. However, the SiGe HBT SPST exhibits larger operational bandwidth, showing that it can be more suitable for broadband applications than the FET SPST. If we consider the 2 dB-

insertion-loss bandwidth, the SiGe HBT SPST and the FET SPST have bandwidths of 36.0 GHz and 25.0 GHz, respectively. The SiGe HBT SPST has better isolation, while the FET SPST is more linear. For biasing, the SiGe HBT SPST consumes an additional 0.2 mA from the 1.5 V supply.

2.1.5 Summary

In this section, SiGe HBT-based RF switches were designed to minimize the impact of SET. By optimizing the electrical configuration of the SPST core, the best SET results were obtained in terms of peak and duration by both TCAD simulations and TPA pulsed-laser single-event effect (PLSEE) experiments. This SPST can be used for various RF applications where the signal propagates in one direction and the backward signal flow is suppressed with high reverse isolation. In addition, the design considerations for SiGe HBT SPST were discussed for the optimal RF performance. The comparison with the conventional FET SPST provides additional information on the trade-offs for optimal SET mitigation strategies and RF performance.

2.2 Radiation-Hardened SiGe-HBT RF Low-Noise Amplifier

2.2.1 Introduction

In most RF wireless systems, an LNA is one of the critical building blocks. Typically, it is the first stage in a receiver RF path and it should provide enough signal gain for the subsequent circuits while adding as little noise as possible to the signal. In addition, for maximum power transfer, the input and the output of an LNA should be conjugate-matched to the impedance of both the preceding and following circuits, respectively.

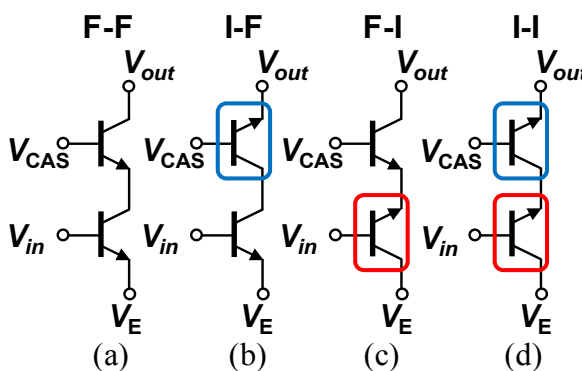


Figure 2.2.1 - Four possible configurations of cascode structures consisting of a CE device at bottom and a CB device at top. (a) forward-forward (F-F), (b) inverse-forward (I-F), (c) F-I, and (d) I-I configurations.

Cascode configuration is the core structure in conventional LNA topologies. It consists of two transistors (Figure 2.1.1 (a)): common-emitter (CE) in series with common-base (CB). The input current signal applied to the base terminal of the CE transistor is amplified at the collector terminal by the current gain (β); the voltage gain of the CE stage in the cascode configuration is approximately equal to unity without degeneration resistors at the emitter. This amplified collector current enters the emitter of the CB transistor and exits the collector with unity gain. The collector current is converted to voltage by the load impedance at the collector of the CB transistor.

From an amplifier perspective, the transconductance (g_m) of the CE stage should be large for a high gain. This makes forward-mode SiGe HBT preferable to inverse-mode. On the other hand, the CB stage can employ an IM SiGe HBT, since it is used as a unity current gain stage in the cascode configuration. Also, the output resistance of the cascode circuit is high; therefore, the overall gain is large. Due to the lower SET sensitivity of the IM SiGe HBT than that of the FM SiGe HBT, the I-F cascode (Figure 2.2.1 (b)) can be utilized in designing SET-mitigated LNAs. In addition, the cascode topology has several advantages over a stand-alone CE amplifier, including increased output resistance (higher voltage gain), reduced Miller capacitance (less unwanted feedback), and increased isolation between input and output terminals (leading to easier matching network design). Thus, it has been widely adopted in many analog and RF amplifiers or multipliers [53], [54].

2.2.2 High-Frequency Performance of IM SiGe HBTs

One can think of four possible combinations for the use of FM or IM SiGe HBTs in cascode configurations as shown in Figure 2.2.1 (a) - (d). Considering the fact that the first transistor stage (CE transistor) determines the overall gain and noise figure (NF) of the cascode structure [55], Figs. 2.2.1 (c) and (d) are not preferred choices, since the reduced current gain and the unfavorably larger capacitive parasitic components in the IM operation will lower power gain and increase minimum noise figure (NF_{min}) of the cascode significantly. However, since the CB stage (Figure 2.2.1 (b)) is used for unity current gain (i.e. no current gain is required), employing an IM SiGe HBT can be a better option for SET mitigation; compared to a conventional forward- forward (F-F) cascode (Figure 2.2.1 (a)), RF performance degradation is minimal.

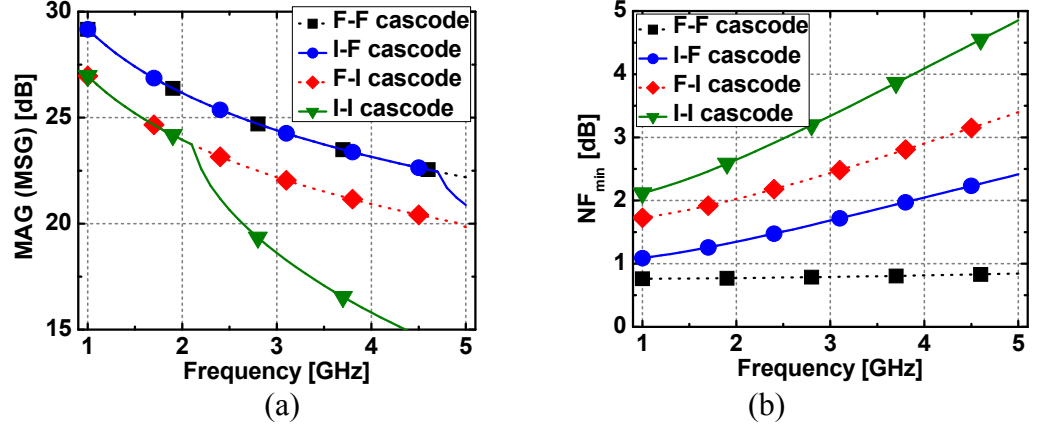


Figure 2.2.2 - (a) Simulated MAG or MSG versus frequency for different cascode configurations. Kinks in the plots are from the stability of cascode cores. (b) NF_{min} versus frequency.

The TCAD simulation results of the gain and noise performance of each cascode topology are shown in Figure 2.2.2. The TCAD model was calibrated for FM operation. The model was not verified for IM at the device level due to the insufficient measurement data for IM SiGe HBTs. However, the close match between the simulation and measurement results of the IM SiGe HBT-based LNA validated the IM simulation results. The maximum available gain or maximum stable gain, an indicator of device stability, is shown in Figure 2.2.2 (a). Both the F-F cascode and the I-F cascode have similar gain until 4.7 GHz, where the I-F cascode becomes stable. When the CE devices are in IM operation (F-I and I-I cascode cores), a gain decrease is noticeable due to reduced current gain of the CE devices. In Figure 2.2.2 (b), the minimum noise figure (NF_{min}) is shown for each cascode core. The I-F cascode has minimal degradation in NF_{min} when compared to the F-F cascode case. On the other hand, the F-I and the I-I cascode cores exhibited significant loss in noise performance in addition to the reduction in gain. Therefore, we will focus on the I-F cascode for the SET-mitigated LNA design.

I-F and the F-F cascode structures exhibited a similar transient duration, whereas the I-F cascode had the smallest transient peak. For the CB strike case with the same ion-strike LET (Figure 2.2.4 (b)), the I-F cascode had better response in terms of both transient peak magnitudes and transient durations. The discussion on these results will be given in the following section.

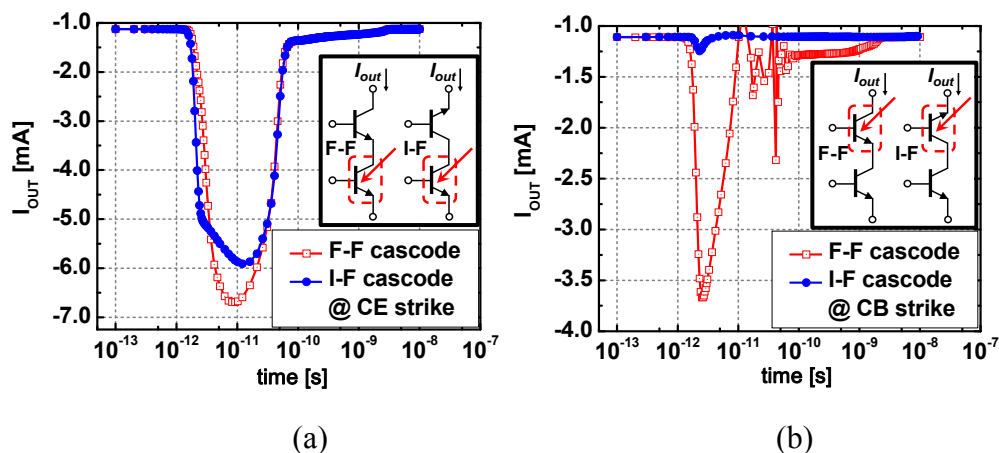


Figure 2.2.4 - Mixed-mode simulation results for SET responses of the F-F and the I-F cascodes under (a) the CE and (b) the CB strike condition. The location of ion strike was the emitter area where the transient peak was highest (see Figure 2.2.3). Each device has a $0.12 \mu\text{m} \times 2.5 \mu\text{m}$ emitter area. The LET was set to $3 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. The CFDRC's NanoTCAD software suite was used.

2.2.4 Pulsed-Laser Experimental Results

The laser-induced SEE experiment was conducted at the U. S. Naval Research Laboratory (NRL) using a through-wafer, two-photon absorption (TPA) technique [20]. The 2-D raster scans were obtained only for the cascode core structures as opposed to the full LNA circuits due to the stability issues arising from the coupling of the wirebond and the test board parasitics. However, since the cascode core structures had the same layout

as in the LNAs and the matching network's response is limited to the bandwidth around the RF signal frequency, the cascode transient should accurately represent the actual LNA response under heavy-ion strikes.

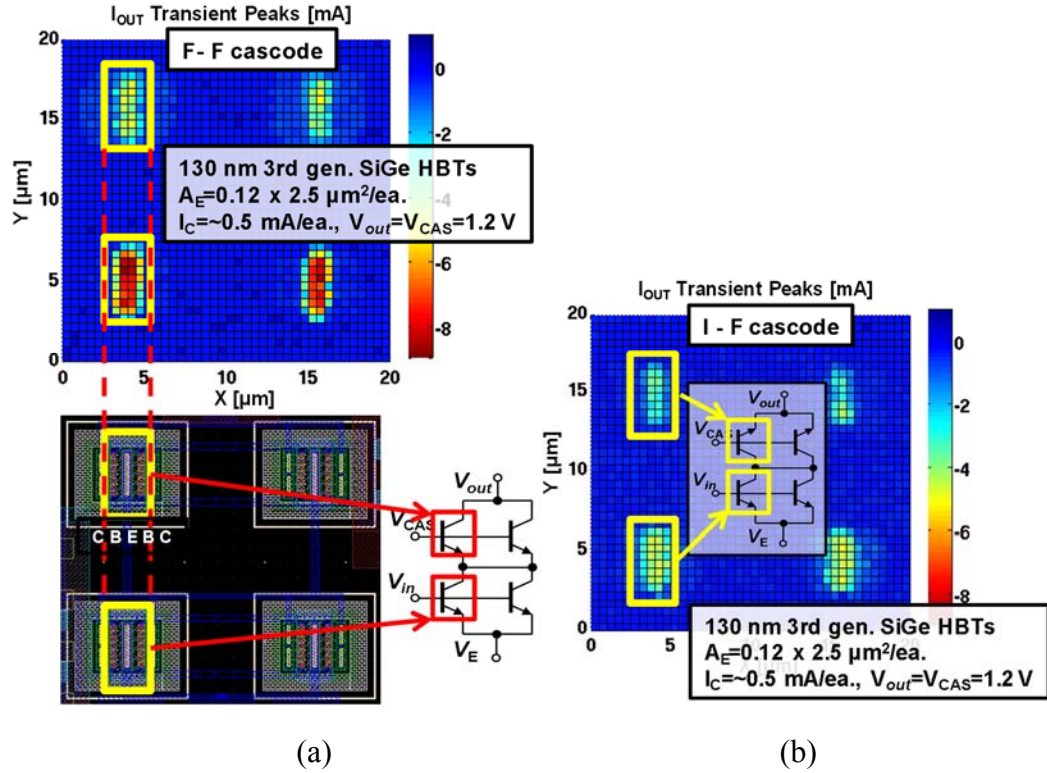


Figure 2.2.5 - Two-dimensional raster scans of (a) F-F and (b) I-F cascode cores. The equivalent layout and the schematic are provided.

The 2-D raster scans detailing the spatial sensitivity for both cascode configurations are shown in Figure 2.2.5. The CE and the CB stages have two parallel-connected SiGe HBTs for better current distribution and impedance matching. The 2-D raster scans are compared to the layout on the same scale (Figure 2.2.5 (a)) and we can see the relative sensitivity of each terminal within the SiGe HBTs. Observe in Figure 2.2.5 (a) that the most sensitive area within the SiGe HBT corresponds to the bulk HBT material stack volume (emitter/base/collector/substrate), which is expected. From this, it can be inferred that a large proportion of the electron-hole pairs were generated in the physical emitter-

base and collector-base junction areas. The CE strike produced larger transient peaks than the CB strike for both the F-F and the I-F cascode cores, since the base-emitter voltage (V_{BE}) of the CE device is the dominant bias that determines the total current of the cascode.

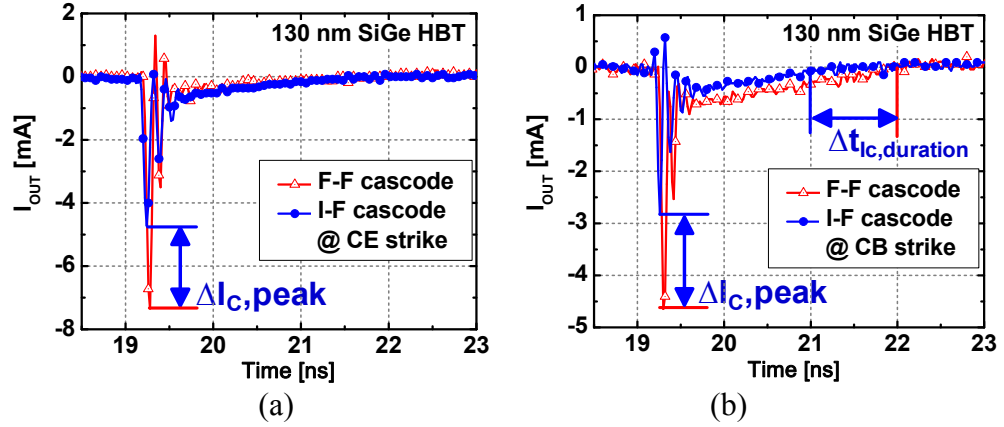


Figure 2.2.6 - Measured output current transient responses of the cascode cores under (a) CE and (b) CB strike with the same laser energy.

From Figure 2.2.5 (a) and (b), the relative difference in the peak transients between the F-F and the I-F cascode cores can be observed. In the CE strike case, the largest portion of the excess electron-hole pairs generated from the CE device will enter the electrical emitter of the CB device. When the CB device is in inverse mode, some of these injected carriers will flow through the substrate-subcollector junction, which helps reduce the output transient peak at the electrical collector. However, when the CB device is in forward mode, most of the injected carriers can pass from the emitter to the collector and hence, the output peaks become larger than for the IM case. In the CB strike case, the I-F cascode had the lowest peaks as well, since the IM SiGe HBT provides greater isolation between the subcollector- substrate diffusion current and the electrical collector terminal [20].

The measured transient peaks versus time are plotted in Figure 2.2.6. Compared with the TCAD simulations (Figure 2.2.4), the relative trends are in qualitative agreement. In the CE strike case (Figure 2.2.6 (a)), the I-F cascode exhibited a reduced peak and a similar transient duration, whereas in the CB strike (Figure 2.2.6 (b)), a reduction in both the transient peak and the duration was observed. There was a slight increase in the transient duration (~ 0.1 ns) for the I-F cascode when the CE was struck. However, the average and the worst-case transient durations were 0.45 and 0.4 ns, respectively, which were shorter than those of F-F cascode.

2.2.5 Reliability Considerations

Reliable device operation under electrical stress conditions is one of the critical factors for long-term system performance. Among a number of possible stress sources, here we focus on the degradation both in current-voltage relationship and high frequency gain from reverse biased junction stress over time.

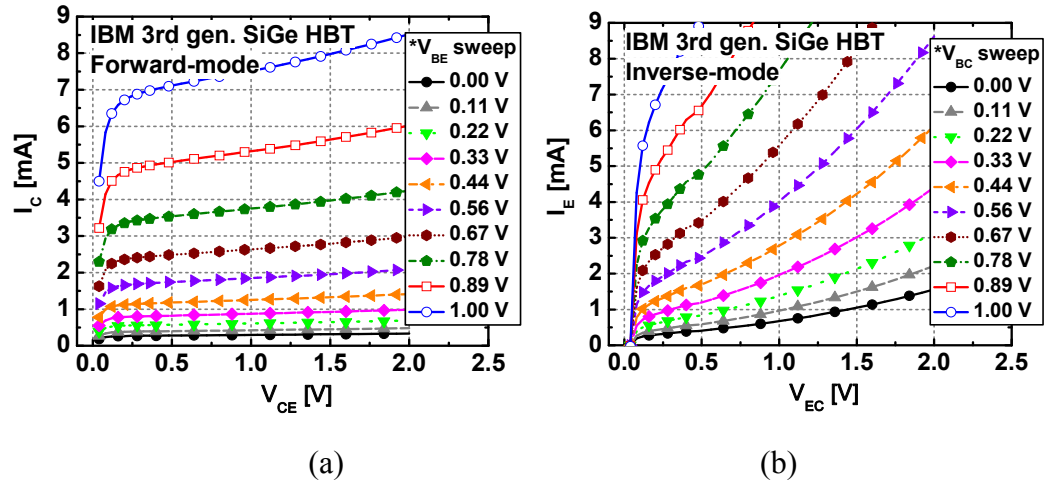


Figure 2.2.7 - Simulated I-V curve for a single IBM 3rd generation SiGe HBT. (a) forward-mode I_C vs. V_{CE} and (b) inverse-mode I_E vs. V_{EC} . Inverse-mode shows much higher output conductance.

First, we need to see the basic I_C versus V_{CE} for FM operation (or I_E versus V_{EC} for IM) without any stress (in Figure 2.2.7). One of the major differences between FM and IM is the device output conductance [50]. This is because in IM operation, the heavy doped emitter (electrical collector) modulates the neutral base width much more than in FM. As a consequence, the change in output voltage now has greater impact on the branch current and the device linearity is inevitably compromised, especially when large-signal operation is required. However, since the typical LNAs operate with small signals, the drawback from large output conductance can be somewhat mitigated.

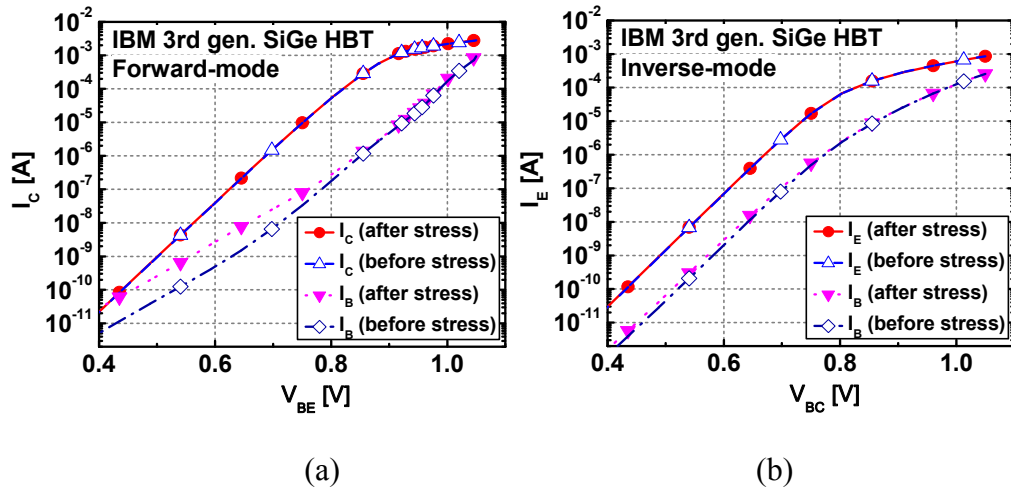


Figure 2.2.8 - Simulated current (I_C and I_B) degradation before and after 10,000 second stress (a) in forward-mode and (b) in inverse-mode operations. $I_C = 2.5$ mA and V_{CB} (or V_{EB} in inverse-mode) = 3.0 V.

The simulated change in the I-V relationship before and after stress is shown in Figure 2.2.8. As expected, the current gain of FM was larger than that of IM [56]. After 10,000 seconds of stress with V_{CB} (or V_{EB} in IM) = 3.0 V, the collector currents remained almost the same as before stress (in both cases). On the other hand, the base currents in

both cases increased after stress as a result of trap generation at the oxide isolation layer. However, the relative change in IM was much less than the FM change.

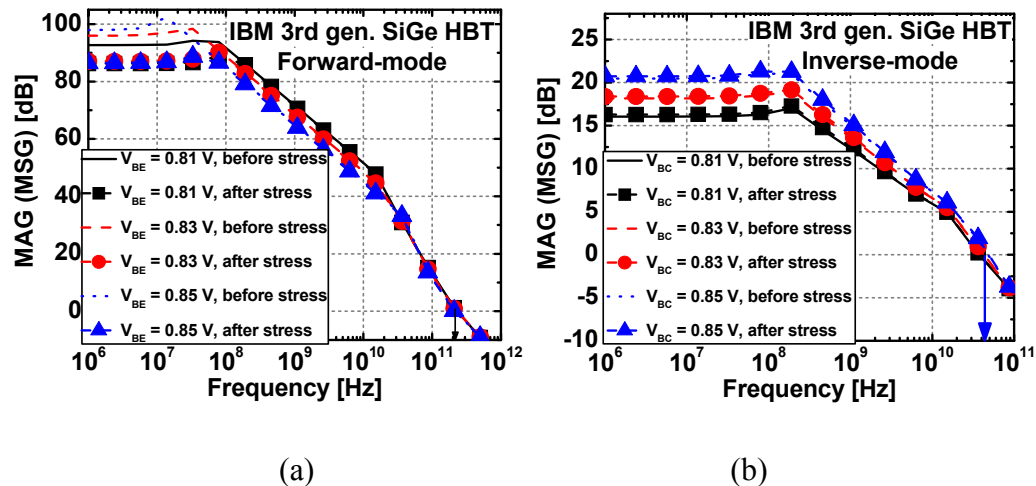


Figure 2.2.9 - Simulated degradation of maximum available gain (MAG) before and after 10,000 second stress (a) in forward-mode and (b) in inverse-mode for different VBE (or VBC in inverse-mode) values. VCB (or VEB in inverse-mode) = 3.0 V.

Figure 2.2.9 shows the simulated gain (MAG) degradation before and after an applied electrical stress of 10,000 seconds under practical bias conditions. In FM operation, the peak f_{MAX} was about 230 GHz when the base-emitter voltage (V_{BE}) was 0.81 V. When the frequency was higher than about 100 MHz, the MAG degradation was negligible, whereas the gain degraded noticeably in the lower frequency region (Figure 2.2.9 (a)). In the case of IM operation (Figure 2.2.9 (b)), the peak f_{MAX} was about 45 GHz, resulting from limited current gain and large parasitic capacitance. Although the RF performance of IM operation is inferior to FM operation, it exhibits more reliable gain characteristics even in the low frequency range (< 100 MHz). These results suggest that IM SiGe HBTs are attractive for broadband, high reliability systems as well as RF applications.

2.2.6 SiGe-HBT RF LNA Design and Discussion

The schematic of the RF LNA is shown in Figure 2.2.10 (a). In the LNA schematic, the inductive degeneration using L_E provides a real impedance to the RF input port and better circuit stability. The external base capacitor (C_B) is for tuning the optimum source impedance and the series inductor (L_B) matches the imaginary part of input impedance. The collector inductor (L_C) and the output capacitor (C_O) are tuned to the center frequency. The collector resistor (R_C) improves stability and can be adjusted for the real part of output impedance. For the performance comparison, both LNAs with F-F cascode and I-F cascode cores were designed and fabricated in IBM 130 nm 8HP platform. The die micrograph of the implemented LNA is shown in Figure 2.2.10 (b). The core area of the LNA was about 0.5 mm^2 ($0.79 \text{ mm} \times 0.63 \text{ mm}$), excluding pads.

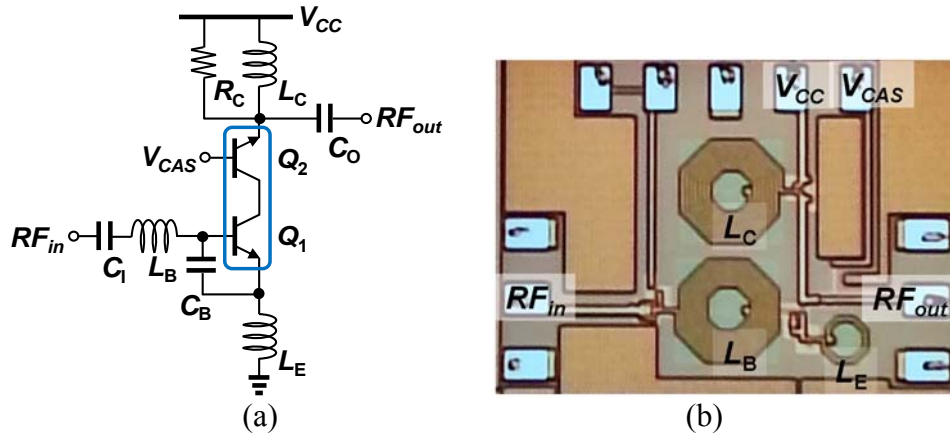


Figure 2.2.10 - (a) Schematic of the proposed I-F cascode LNA. It consists of a cascode and input and output matching networks tuned at 2.4 GHz. (b) Die micrograph of the I-F cascode LNA.

In Figure 2.2.11, the measured S_{21} (forward power gain) and noise figure (NF) are plotted against frequency. The I-F LNA had an RF gain (S_{21}) of 23 dB and it is only 1 dB

less than that of the conventional F-F LNA. The LNA input and output were matched at 2.4 GHz and 2.5 GHz and the return loss at the matched frequencies were 18 dB and 13 dB, respectively (not shown here). The NFs of the two LNAs were also similar (~2.4 dB) at 2.4 GHz. As the frequency moves further from the center frequency toward either end of the operational frequency band, the I-F LNA typically had 0.2~0.4 dB higher NF.

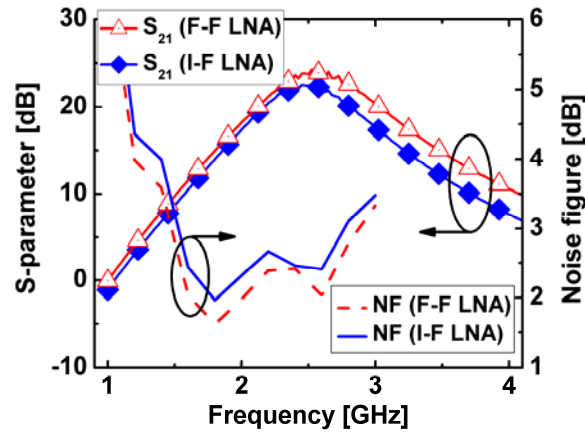


Figure 2.2.11 - Measured S_{21} (forward power gain) and noise figure (NF) of both the F-F LNA and I-F LNA versus frequency.

Table 2.2.1 - LNA Performance Summary

LNA core structure	I-F cascode	F-F cascode	I-I cascode*
f_0 [GHz]	2.4	2.4	2.4
S_{21} [dB]	23	24	11
NF [dB]	2.5	2.4	4.7
P1dB [dBm]	-22	-20	-12
P _{DC} [mW]	1.8	1.8	1.7

*The I-I cascode LNA had neither inductive degeneration (L_E) and nor external base capacitor (C_B) to obtain higher gain (S_{21}) as much as possible since the MAG was around 30 GHz.

Table I summarizes the RF performance parameters for the LNAs fabricated with the various cascode structures. The proposed I-F cascode-based LNA has similar performance to the conventional F-F cascode LNA. For a more complete comparison, the LNA with the I-I cascode (Figure 2.2.1 (d)) was also included, even though its expected performance is modest. As mentioned earlier, the gain and the noise performance of the I-I cascode LNA were far inferior to the other two LNAs (Figure 2.2.2).

2.2.7 *Summary*

In this work, a radiation-hardened RF LNA was designed using IM SiGe HBTs in a 130 nm SiGe platform, demonstrating the potential capability of the IM SiGe HBT in space-based RF applications for the first time. We have shown that the proposed LNA provides good RF performance compared to the standard LNA, and a partially mitigated sensitivity to SET. To verify the radiation tolerance of the proposed LNA, the F-F and I-F cascode cores were characterized using pulsed-laser TPA. The resulting transient responses confirm a significant reduction in the output current peak magnitudes and durations. These results were supported by mixed-mode TCAD simulations. Additional investigations on the RF performance and the reliability of the IM-based cascode configuration further substantiate the feasibility of the proposed cascode cores in RF LNA designs for space environments.

2.3 Investigation of the Use of Inverse-Mode SiGe-HBTs in RF Mixers

2.3.1 Introduction

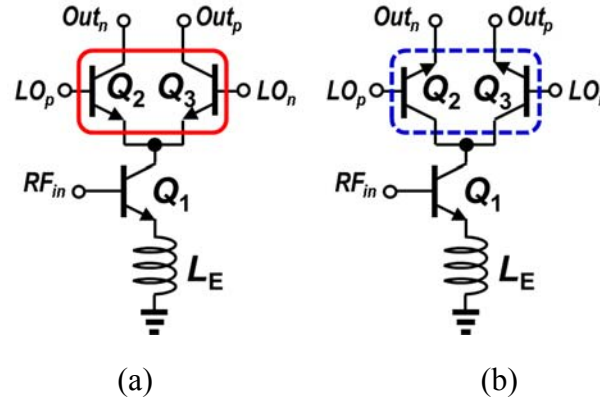


Figure 2.3.1 - Mixer core schematics with (a) FM SiGe HBT differential pair and (b) IM SiGe HBT differential pair.

The core schematic of a conventional single-balanced, down-conversion mixer is shown in Figure 2.3.1 (a) [55]. The input RF signal is applied at the base terminal of Q_1 . To match the impedance between the signal source and the RF input transistor Q_1 , a degeneration inductor is typically connected between the Q_1 emitter and ground in order to present real impedance ($50\ \Omega$) at the input. The switch pair (Q_2 and Q_3) is driven differentially by LO signals and the magnitude of the LO signals are large enough to completely steer the branch current between Q_2 and Q_3 , in contrast to an analog differential amplifier. This switching operation performs frequency translation, and consequently, generates differential IF outputs at the collector nodes of Q_2 and Q_3 by mixing the LO and RF signals. Conventionally, resistive loads at the collector terminals of Q_2 and Q_3 are used to provide conversion gain.

As mentioned above, in an ideal mixer, the role of a switch pair is to fully turn on one transistor of the differential pair and turn off the other for higher conversion gain and low noise operation [55]. Since the differential pair transistors do not need high gain (transconductance, g_m), but require full switching, there is some room for IM SiGe HBTs to replace FM SiGe HBTs for SET mitigation under heavy-ion strike, as indicated in Figure 2.3.1 (b). With the help of technology scaling, the IM SiGe HBT has become a more suitable candidate for low GHz operation [20], [23]. By utilizing the IM SiGe HBTs to replace the switching pair (Figure 2.3.1 (b)), the SET response of both FM and IM switch pairs in RF mixers can be compared and analyzed.

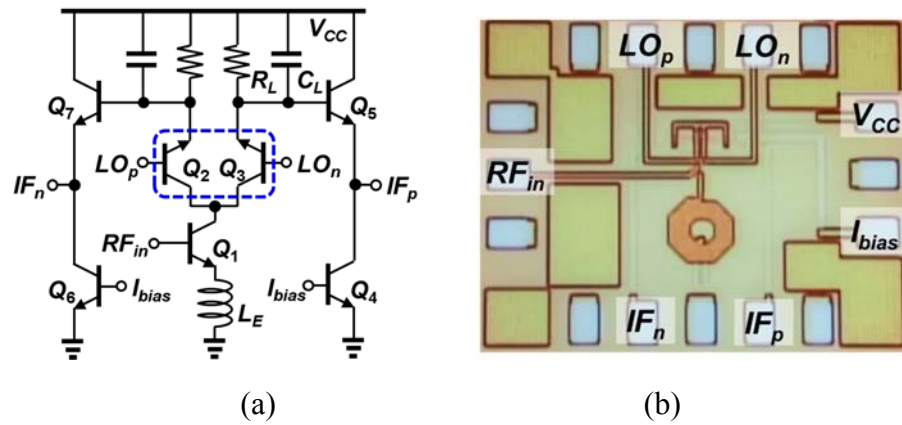


Figure 2.3.2 - (a) Full schematic of a down-conversion mixer with IM SiGe HBT differential pair. (b) A chip micrograph of the fabricated circuit.

2.3.2 Design of RF Mixer with Inverse-Mode SiGe HBTs

The full schematic of the SiGe HBT RF mixer is shown in Figure 2.3.2 (a). While the same mixer core is used, some components are added for performance optimization and measurement purposes. In order to filter out the unwanted up-converted frequency

components, load capacitors (C_L) are added in parallel with load resistors (R_L) at the electrical collector terminals of the differential pair. For decoupling the load impedance at the mixer core from the instrument loading and prevent gain decrease, an emitter-follower (EF) buffer stage (Q_5 and Q_7) was inserted between the mixer core and the monitoring terminal. Due to its $1/g_m$ output impedance, the EF stage can easily match the circuit impedance to the instrument. The chip micrograph is shown in Figure 2.3.2 (b). Except for an RF feed metal line and DC biasing circuitry, the layout was designed to be as symmetric as possible to suppress even-order distortion. The total chip area was about 0.91 mm^2 ($1.08 \text{ mm} \times 0.84 \text{ mm}$).

2.3.3 TCAD Model Set-up and Simulation

A 2-D TCAD model was developed and implemented in a Sentaurus environment [57] for IBM 8HP SiGe HBTs. With the calibrated TCAD model, the responses of SiGe HBTs under heavy-ion strikes were simulated. The value of linear energy transfer (LET) used in the simulations was $2 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. 0.85 V was applied to the base of Q_1 , resulting in about 0.8 mA of collector current. 1.9 V and 2.5 V were applied to the base and the collector terminals of the switching pair (Q_2 and Q_3), respectively. In the TCAD simulation, ideal resistors (R_L) and capacitors (C_L) were inserted between the collector terminals (of Q_2 and Q_3) and V_{CC} to bias the mixer core transistors and provide load impedance to the differential pair. The values of the R_L and the C_L were 700Ω and 240 fF , respectively.

For heavy-ion strikes on the RF device Q_1 , the resulting output transient waveforms are shown in Figure 2.3.3 (a). The IM SiGe HBT core exhibits reduced peak and faster recovery at the beginning, compared to the FM SiGe HBT differential pair. The different

transients between the FM and the IM can be explained with the base transient currents of Q_2 (and Q_3). Since the base bias of Q_1 and the resulting collector currents in both the FM and the IM cores were the same, the excess carriers generated during the ion-strike should be the same. By comparing the base transient waveforms in Figure 2.3.3 (b), it implies that in the FM case, most excess carriers are supplied from the collector terminal of Q_2 (and Q_3), while in the IM core the excess carriers are supplied from both the base and the collector of Q_2 (and Q_3). Hence, the IM core exhibits a less sensitive transient at the electrical collector but a more sensitive transient at the base terminal. Since the total transient duration is mainly limited by the electrical collector transient, however, the longer base transient does not degrade the overall duration of the IM mixer core. In addition, these base transients will not significantly disturb stable bias condition due to the large impedance placed in a DC path and the small impedance in an AC path. On the other hand, the impact of substrate transients can be ignored due to their relatively small responses compared to the base transient currents (Figure 2.3.3 (b)).

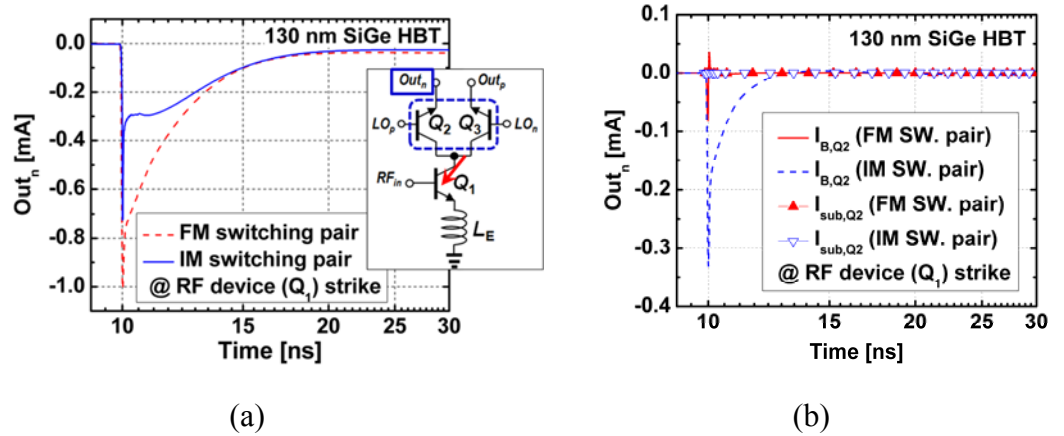


Figure 2.3.3 - Heavy-ion TCAD simulation results. (a) Output current transients when ion strikes the RF device (Q_1). (b) Transient currents at the base and the substrate terminals of LOP (Q_2) device.

Figure 2.3.4 (a) shows the SETs when the heavy ion strikes Q_2 . Similarly, the IM SiGe HBT differential pair exhibits smaller peaks and shorter durations. In Q_3 strike cases (Figure 2.3.4 (b)), the overall advantages of IM SiGe HBTs are maintained in terms of transient peaks and durations. The difference in SET response between the FM and the IM SiGe HBTs are described more in detail in the next section. Since the total current of the differential pair remains constant due to fixed voltage biasing of Q_1 , the SET current at Q_3 will be mirrored at Q_2 with opposite polarity.

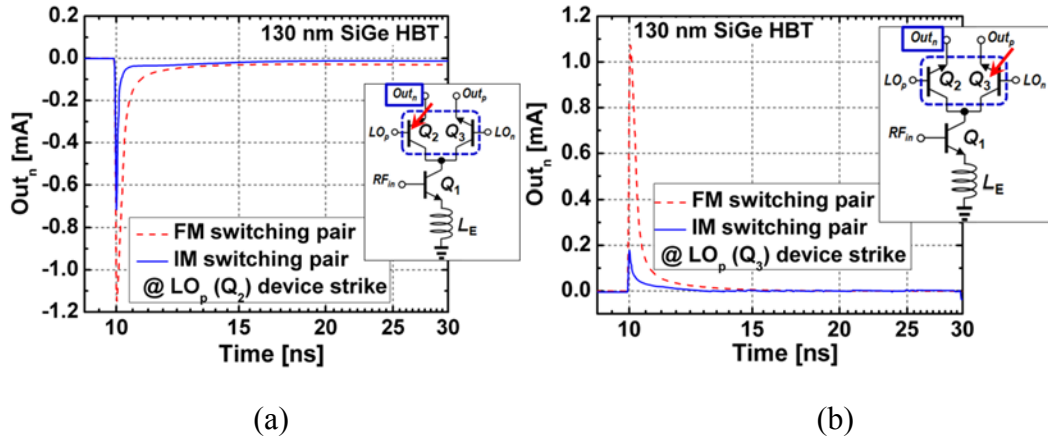


Figure 2.3.4 - Output current transients at the Outn terminal when ion strikes the (a) LOp device (Q_2), and (b) LOn device (Q_3).

The heavy-ion TCAD simulation results with different LET values are shown in Figure 2.3.5. Since orbital environments have heavy ions with LET close to tens of $\text{MeV}\cdot\text{cm}^2/\text{mg}$ [58], it is important to see how the FM and IM SiGe HBTs behave under a high energy ion strike. The Q_2 collector current transients were monitored when Q_2 was struck. For low LETs below 10, the IM mixer core exhibited reduced peak and shorter duration than the FM core. On the other hand, with LETs higher than $20 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, the IM mixer core showed higher peaks while maintaining shorter durations. Therefore, IM

SiGe HBTs require further reliability consideration especially for heavy ion strikes with high LETs.

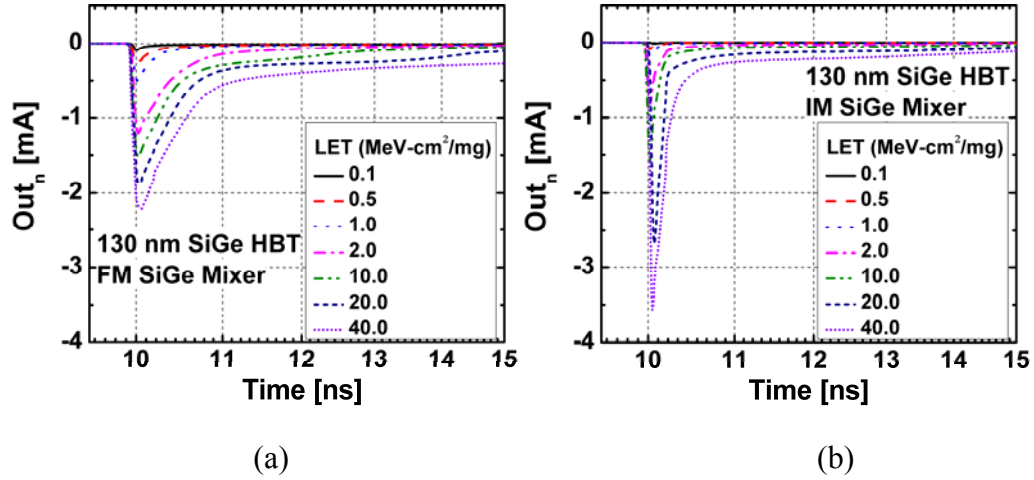


Figure 2.3.5 - Heavy-ion TCAD simulation results with different LETs for (a) FM and (b) IM SiGe HBT mixer cores. The collector currents of Q_2 were monitored when Q_2 was struck.

In order to explore full current-steering conditions, the SET responses when the differential pair was fully ON and OFF were simulated (Figure 2.3.6). Since the LO signal is fixed at the DC biasing state, the dynamic response cannot be observed. However, the relative peaks and durations can be monitored. For the ON (Figure 2.3.6 (a)) and OFF (Figure 2.3.6 (b)) states, 2.2 V and 1.6 V were applied to the base of Q_2 , respectively. Compared to an equal biasing state as in Fig. 6, the peaks were relatively smaller and the transient durations were shorter. In both ON and OFF states, the IM mixer core showed reduced peaks and shortened durations. Based on these preliminary simulation results, it is observed that the IM SiGe HBTs offer advantages for mitigating the impact of ion-strikes in mixers.

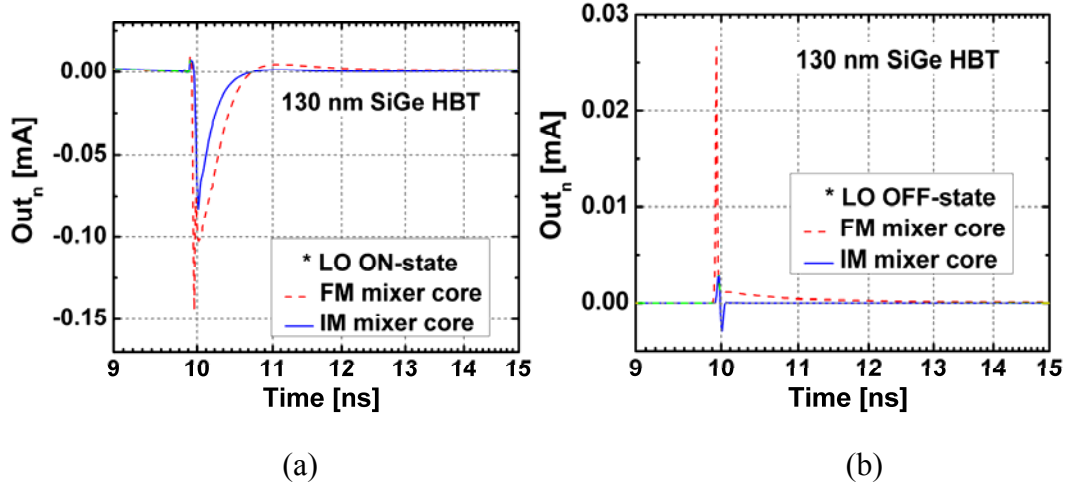


Figure 2.3.6 - Heavy-ion TCAD simulation results when a differential pair is fully (a) ON or (b) OFF. Q_2 collector current was monitored for FM and IM mixer cores.

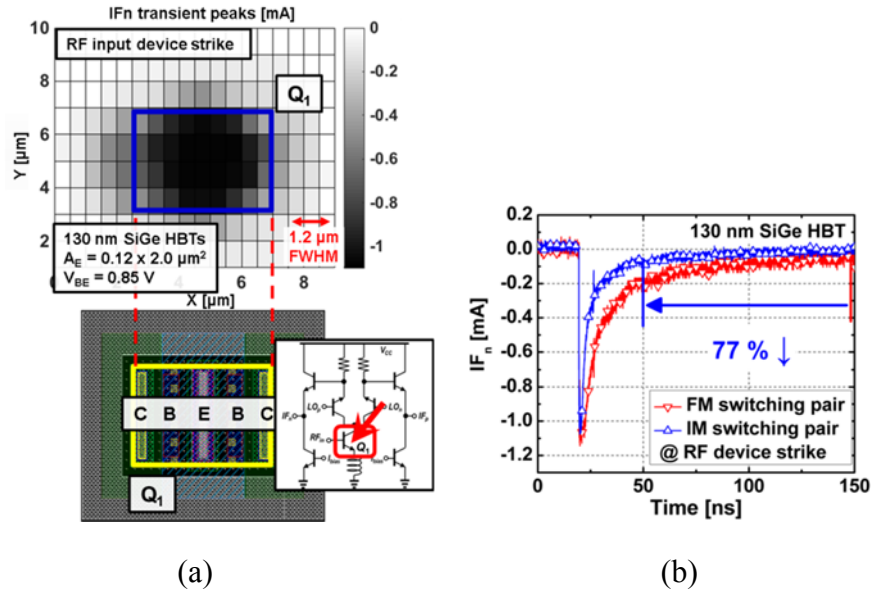


Figure 2.3.7 - (a) 2-D raster scan at the IFn terminal of the mixer with the IM SiGe HBT switching pair under RF input device (Q_1) strike. (b) Time domain SET response of both mixers.

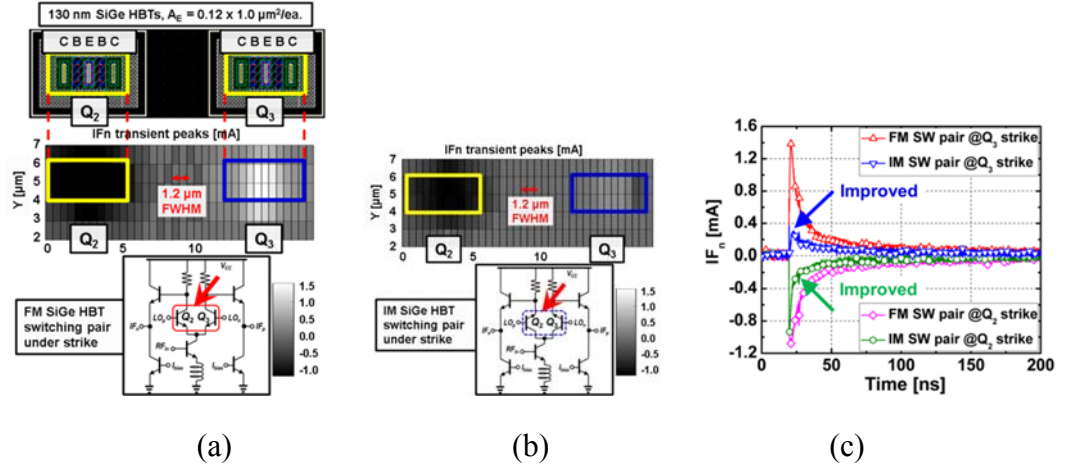


Figure 2.3.8 - Two-dimensional raster scan at the IFn terminal under the switching pair strike for (a) FM and (b) IM SiGe HBT mixers. (c) Time domain SET responses of both FM and IM SiGe HBT mixers.

2.3.4 TPA Pulsed-Laser Beam Experiment Results

In order to characterize the SETs of the FM and the IM SiGe HBT mixers, a laser experiment was conducted at the Naval Research Laboratory (NRL). A through-wafer, two-photon absorption technique was used to generate a laser-beam with 150 fs pulse duration at a wavelength of 1.26 μm and 1.2 μm full width at half maximum (FWHM) spot size [47], [48]. To drive LO_p and LO_n with differential LO signals and DC common-mode biasing, a balun and bias tees were connected together. The differential outputs (IF_n and IF_p) were separately measured to check if there were any abnormal differences between them. The laser energy used throughout the experiment was about 3.45 pJ. Since, in general the correlation between laser energy and heavy ion LET is non-linear and dependent on the technology of interest [59]-[62], the accurate equivalent LET needs further characterization. Based on [59]-[61], it is expected that the equivalent LET will be located between approximately 1 and 10 MeV·cm²/mg.

Figure 2.3.7 (a) shows the 2-D raster scan of the IM SiGe HBT mixer for the RF device (Q_1) strike, at DC conditions. As expected, the SET responses of the two output terminals (IF_n and IF_p) were very close to each other (not shown here). With the actual transistor layout, the sensitivity of each point can be mapped from the raster scan. Black and white points represent the highest and the lowest sensitivity on the pulsed-laser, respectively. The emitter stripe was the most sensitive region since all junctions (EB, CB, and collector-substrate) were vertically stacked. In Figure 2.3.7 (b), the time domain SETs of both the FM and the IM SiGe HBT mixers are compared. Both the FM and the IM mixers showed similar transient peaks, while the IM SiGe HBT pairs exhibited a 77% reduction in transient duration for 90% recovery time.

In Figure 2.3.8 (a) and (b), the 2-D raster scans of the IF_n terminal under the switching pair (Q_2 and Q_3) strike are shown. The strike on the Q_2 and Q_3 devices generates transients having different polarities, as shown in Figure 2.3.4. For the Q_2 strike, the AC voltage of Q_2 's (electrical) collector node will be lower than the DC bias level due to the ion-shunt effect [19], [20], showing negative transients. On the other hand, for the Q_3 strike case, the ion-shunt of Q_3 will raise the AC voltage of Q_2 's (electrical) emitter node. Hence, Q_2 's (electrical) collector node voltage will increase since the Q_2 is in a common-base configuration. Figure 2.3.8 (c) shows time domain transients for both the FM and the IM mixers. During the measurement, the most sensitive points along the X, Y and Z axes were found in the transistor area separately for each mixer to represent the worst case responses. The IM mixer showed reduced peaks and shortened durations as expected from the TCAD simulations (Figure 2.3.4). In summary, the IM SiGe switching pair effectively reduces both the SET peaks and durations when compared with the FM switching pair.

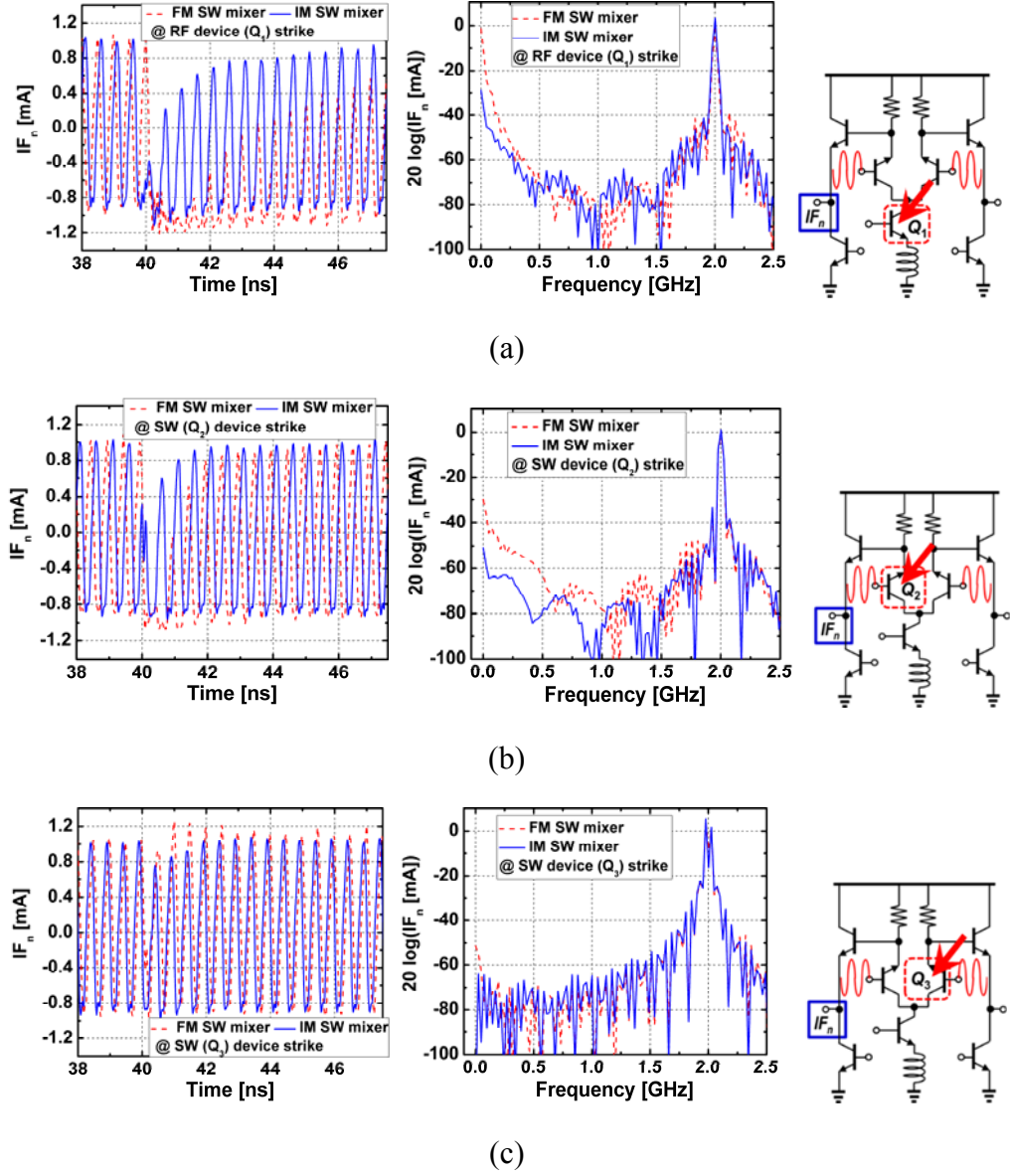


Figure 2.3.9 - Time and frequency domain responses at the IF_n terminals of both the FM and the IM SiGe HBT mixers under: (a) RF input device (Q_1), (b) Q_2 , and (c) Q_3 strikes when the 2 GHz LO signal is applied.

Figure 2.3.9 shows the SET response in both time and frequency domains when the switching pairs are driven by large LO signals. The LO signal has 2 GHz frequency and 0 dBm RF power to reflect a typical large-signal operational condition. In the frequency

spectrum, the highest peaks were observed at 2 GHz which were a feedthrough leakage of 2 GHz local oscillator (LO) signals to the output. In most receiver systems, these peaks will be attenuated or cut off by inserting low pass filters after mixers for subsequent signal processing. Since typical IF bands are in the kHz or MHz range, SET-induced distortion in these bands can corrupt signal integrity or desensitize the receiver [55]. To simplify the analysis, no RF signal was applied at the input, since typical RF input power is much smaller than the LO power. If the RF signal is applied, the frequency of the output envelope signal will be the IF frequency.

In Figure 2.3.9 (a), the relative peaks and duration for FM and IM SiGe HBT mixers when Q_1 was under strike are in accordance with the DC bias condition results (Figure 2.3.7 (a) and (b)). The IM mixer shows SETs of shorter duration and smaller peaks. In the frequency spectrum, low frequency (< 300 MHz) components (spurs) are reduced in the IM switch mixer by average of 20 dB. This is a promising result for the IM SiGe HBT, since typical IF frequency bands are on the order of hundred MHz or less, meaning the overall signal integrity will be improved. Figure 2.3.9 (b) also shows a similar trend from the DC bias condition results: a reduced transient duration and peak when Q_2 was struck. The low frequency components (< 1 GHz) in the frequency spectrum are reduced significantly. Hence, the IM SiGe HBTs can improve signal quality under heavy-ion strike for receivers which use an intermediate frequency (IF) band close to DC [55], [63]. On the other hand, note that the SET response for the IM switch under the Q_3 strike (Fig2.3.9 (c)) exhibits a different trend when compared with DC condition results: the polarity of SET is negative with the large LO signal. In the frequency spectrum, the difference between the FM and the IM switch is less noticeable, except at DC.

Therefore, based on these results, it is concluded that the IM SiGe HBT differential pair in a down-conversion mixer can generally mitigate the impact of transients. It exhibits less distortion and shorter duration in the time domain. In addition, in the frequency domain, the IM SiGe HBTs contribute to lower spurs at the output, especially in the IF band. Along with the reduced peaks and faster recovery in the time domain, these spur reductions can be critical benefits in real time systems. The RF performance of both the FM and the IM SiGe HBT mixers are summarized in Table 2.3.1.

Table 2.3.1 - RF Mixer Performance Summary

Mixer switch pair configuration	Forward-mode SiGe HBT	Inverse-mode SiGe HBT
RF/LO/IF frequency [GHz]	2.4 / 2.0 / 0.4	
conversion gain [dB]	10.6	7.0
noise figure [dB]	10.7	20.6
Receiver noise figure (LNA+mixer)* [dB]	2.1	2.9
P1dB [dBm]	-25	-21
IIP3 [dBm]	-12	-9
P _{DC} (core only) [mW]	2.0	2.0

* For the receiver NF calculation, it is assumed that 1) the LNA has a gain of 25 dB and a noise figure of 2 dB and 2) both the LNA and the mixer have perfect 50 Ω terminations at the inputs and the outputs.

2.3.5 Summary and Implications

An active down-conversion mixer with an IM SiGe HBT differential pair was designed and fabricated in order to investigate the IM SiGe HBT's capability of SET

mitigation under large-signal RF operational conditions. The SET responses of FM- and IM-based mixer cores were obtained by both heavy-ion TCAD simulations and two-photon absorption pulsed-laser beam experiments. The IM SiGe HBT differential pair exhibits smaller transient peaks and shorter duration in both steady state and LO injection conditions (50 % duration reduction in the best case). With respect to RF performance, the IM SiGe HBT mixer has a degraded NF compared to the FM counterpart, and thus in order to compensate the unwanted NF degradation, a high gain LNA is necessary for RF system implementation.

2.4 Design of Radiation-Hardened SiGe-HBT Receiver

2.4.1 Introduction

The core function of general RF receivers is to down-convert the input RF signals to the intermediate frequency (IF) for subsequent data processing. In the operation of frequency conversion, receivers should provide signal-path selection, amplification of the input signal, and mixing the amplified input signal with a local oscillator (LO) signal at the RF switch, LNA, and mixers, respectively [55]. When it comes to the operation in an SET-intensive environment, receivers additionally require minimized susceptibility to SETs in terms of transient peaks and durations. For more in-depth understanding of SET response, it is critical to investigate 1) the effect of a laser (or heavy-ion) strike on each constituent transistor to overall receiver operation and 2) tradeoffs between RF receiver performance and SET mitigation. However, since few studies have addressed these issues related to the use of IM SiGe HBTs in RF receivers, we designed various receiver prototypes which selectively include SET-hardened RF sub-circuits.

This work presents the relative SET responses between a conventional receiver and SET-mitigated receivers, in which IM SiGe HBTs are utilized in switches, LNAs, and mixers. The receivers have the RF and the differential LO signals as inputs and the differential IF of 200 MHz as outputs. Section 2.4.2 will explain the design of receivers with radiation-hardening-by-design (RHBD) techniques and compare the RF performance of each receiver. Section 2.4.3 will show the experiment set-up and the results of a two-photon-absorption (TPA) pulsed-laser SET test and discuss the effect of using of IM SiGe HBTs in RF receivers. Section 2.4.4 will summarize the section.

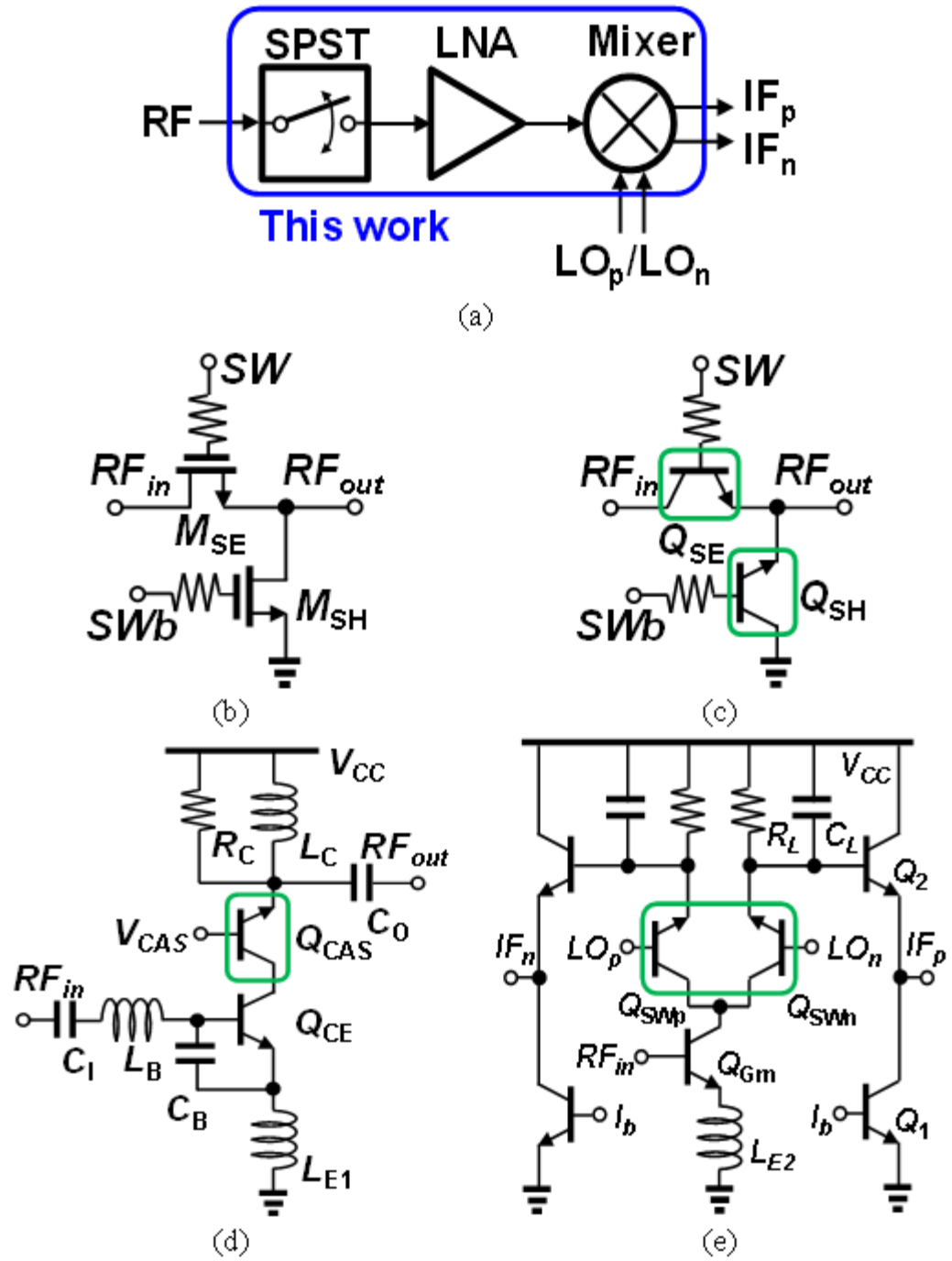


Figure 2.4.1 - (a) Configuration of the RF receiver prototype. (b) Conventional FET-based RF single-pole single-throw switch. (c) RHBD SiGe HBT-based RF switch. (d) RHBD LNA with an inverse-mode (IM) SiGe HBT cascode transistor. (e) RHBD down-conversion mixer with an IM SiGe HBT switching pair.

2.4.2 Design of SET-Mitigated Receivers

The configuration of a receiver prototype is shown in Figure 2.4.1 (a). It includes a single-pole single-throw (SPST) switch, an LNA, and a mixer. Since the mixer is single-balanced, it accepts single-ended RF input and produces a differential output at IF [55]. The schematics of a conventional FET-based switch and the SET-mitigated switch with IM SiGe HBTs are shown in Figure 2.4.1 (b) and Figure 2.4.1 (c), respectively [64]. For LNAs, a conventional topology will use both FM SiGe HBTs in a cascode configuration, while the SET-hardened LNA utilizes an IM SiGe HBTs for the top common-base (CB) transistor (Figure 2.4.1 (d)) [23]. Similarly, the SET-mitigated mixer uses IM SiGe HBTs for a switching pair for mixing operation instead of FM SiGe HBTs (Figure 2.4.1 (e)) [65].

Table 2.4.1 - RF Receiver Configuration

Receiver	Switch	LNA	Mixer
RX1	Conv. FET	Conv. FM SiGe (F-F cascode)	Conv. FM SiGe switching pair
RX2	RHBD w. SiGe	Conv. FM SiGe (F-F cascode)	Conv. FM SiGe switching pair
RX3	RHBD w. SiGe	RHBD w. IM SiGe (I-F cascode)	Conv. FM SiGe switching pair
RX4	RHBD w. SiGe	RHBD w. IM SiGe (I-F cascode)	RHBD w. an IM SiGe switching pair

In this study, inverse-mode SiGe HBTs are applied for non-active gain stages, since RF performance degradation seen as both a gain decrease and a noise figure (NF) increase will be severe due to the reduced current gain and unity gain frequency (f_T) associated with

inverse-mode SiGe HBTs. Therefore, Q_{CE} in the LNA (Figure 2.4.1 (d)) and Q_{Gm} in the mixer (Figure 2.4.1 (e)) are kept as FM SiGe HBTs. Instead, IM SiGe HBTs are used for passive circuits (series/shunt transistors in RF switches), current buffers (cascode CB transistors in LNAs), and switching pairs in mixers with reasonable performance degradation for SET mitigation.

Table 2.4.1 summarizes the configuration of four receivers. RX1 is a conventional receiver with a standard FET-based switch and an all-FM SiGe HBT-based LNA and mixer. RX2, RX3, and RX4 sequentially replace each component with an SET-mitigated circuit. Thus, the impact of each circuit with RHBD techniques can be compared for SET-mitigation as well as RF performance.

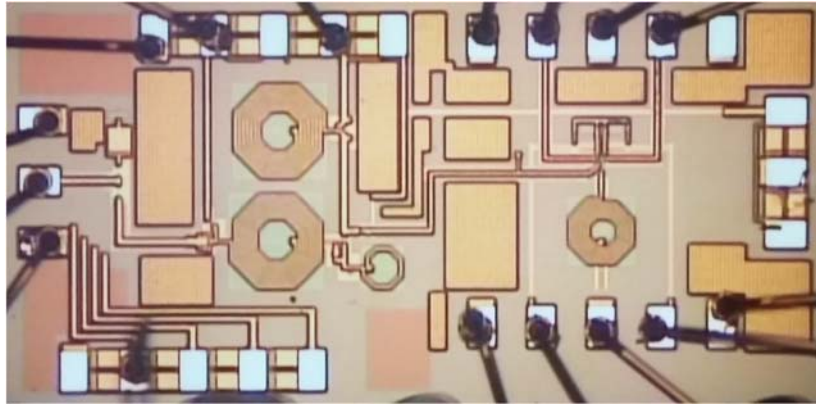


Figure 2.4.2 - Chip micrograph of a receiver prototype. The chip size is 1 mm x 2 mm, including measurement pads.

2.4.3 Experimental Results and Discussion

The receiver prototypes were designed and fabricated in a GlobalFoundries 130 nm 8HP BiCMOS technology platform. The chip micrograph of RX4 is shown in Figure 2.4.2. The RF performance parameters of each receiver are summarized in Table 2.4.2. Since IM SiGe HBTs have much lower f_T (~ 20 GHz) than FM SiGe HBTs (220 GHz), the use of IM SiGe HBTs in RF circuits results in degradation of receiver performance. The tendencies of gain decrease and NF increase are observed from RX1 to RX4.

Table 2.4.2 - RF Performance Summary

Perf. Parameter	RX1	RX2	RX3	RX4
RF/LO/IF [GHz]	2.4/2.0/0.2			
Conversion gain [dB]	26.8	25.1	23.8	20.4
Noise figure [dB]*	9.0	10.6	11.1	14.5
IP1dB [dBm]*	-29.0	-28.1	-26.6	-26.1
DC power [mW]	18.7	19.0	19.0	19.0

* Simulation results

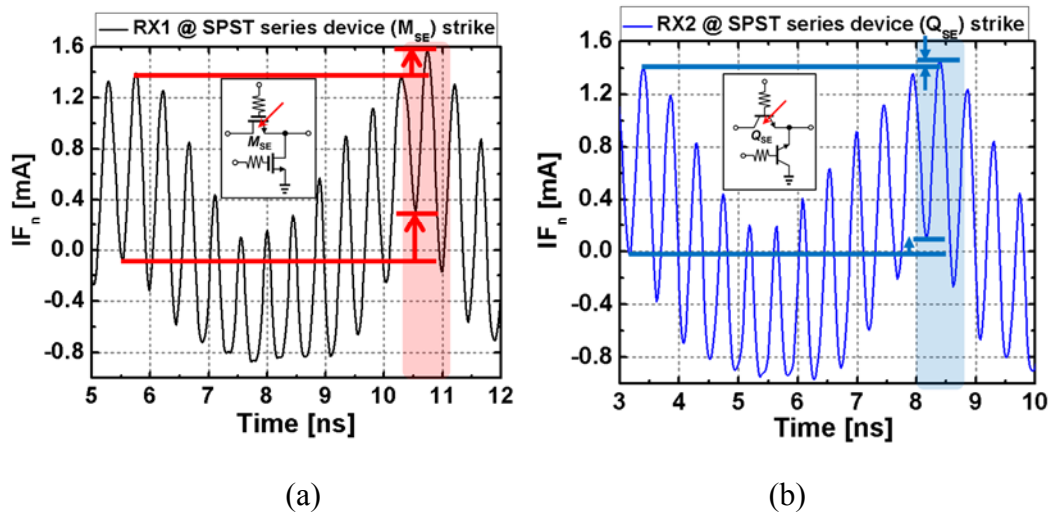


Figure 2.4.3 - Output time domain SET response when the laser beam strikes series devices of RF switches in (a) RX1 and (b) RX2. The outputs were measured at the mixer output port IF_n .

A through-wafer TPA pulse-laser experiment [48] was conducted at the US Naval Research Laboratory (NRL) for measuring the resultant transient waveforms for the receivers. The generated laser-beam had pulse duration of 150 fs, wavelength of 1.26 μm , and full width at half maximum (FWHM) spot size of 1.2 μm . The receiver chips were attached to custom-designed high speed printed circuit boards and wire-bonded for biasing and RF signals. In order to fully capture high-frequency transients, a high-speed oscilloscope (Tektronix DPO 71254) was connected to the signal lines through bias tees.

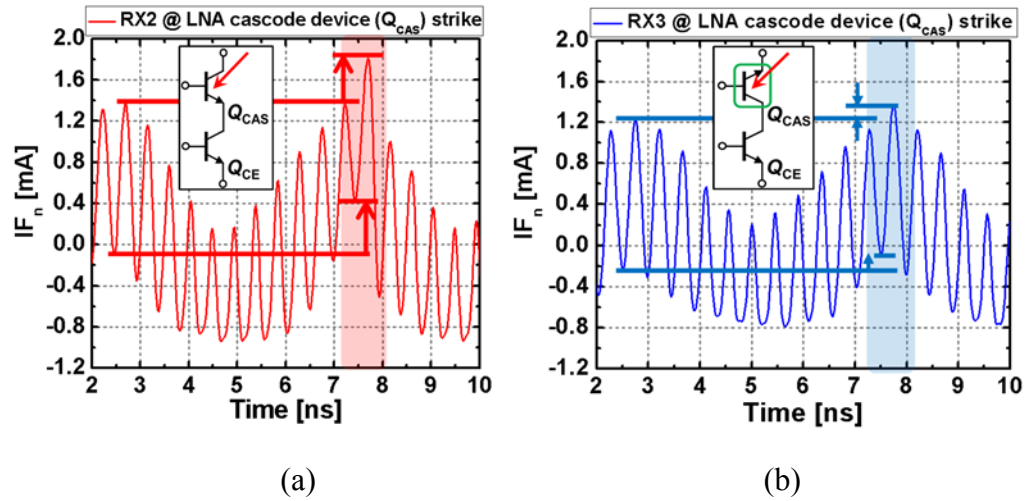


Figure 2.4.4 - Output time domain SET response when the laser beam strikes common-base transistors (Q_{CAS}) of LNA cascode branches in (a) RX2 and (b) RX3. The outputs were measured at the mixer output port IF_n .

The measured SETs of RX1 and RX2 when the laser beam strikes a series device in switches are shown in Figure 2.4.3. All waveforms were measured at the mixer output port IF_n . The laser beam was focused along the emitter stripes and then varied in the Z-direction in order to maximize the SET response. Since the series devices of switches exhibit larger

peaks than the shunt devices, only the SETs of series device strikes are shown in Figure 2.4.3 (a) and (b). RX1, which includes an FET-based switch, shows more distortion in the envelope signal than RX2 with a SiGe HBT-based switch [64]. Even though in both cases the durations of SETs are similar, about two LO cycles, the distortion in envelope signal may cause degradation of signal-to-noise ratio (SNR) or data loss.

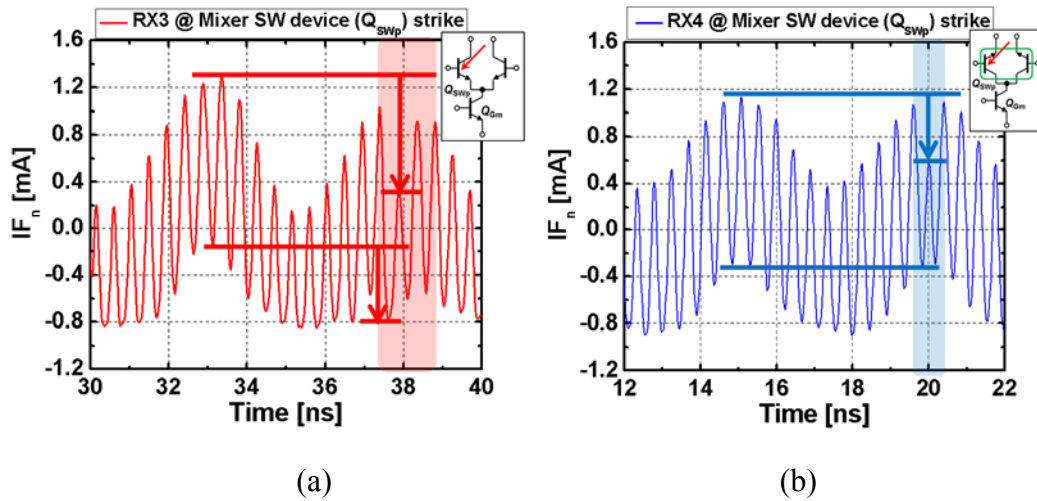


Figure 2.4.5 - Output time domain SET response when the laser beam strikes switching pairs of mixers in (a) RX3 and (b) RX4. The outputs were measured at the mixer output port IF_n .

In Figure 2.4.4, the measured SETs of RX2 and RX3 at the IF_n terminal when the laser strikes the CB transistors (Q_{CAS}) of the LNAs are shown. The overall SET response is the peak change (or distortion) in the envelop signals, while the duration is about two LO cycles for both the FM and IM SiGe HBT cases. However, RX3, which uses an IM SiGe HBT in the cascode configuration (Figure 2.4.4 (b)), exhibits much smaller peak changes at the mixer output than RX2 (Figure 2.4.4 (a)) [23].

The measured SETs of RX3 and RX4 when the laser beam strikes one of a switching pair (Q_{swp}) are displayed in Figure 2.4.5. RX3, which includes FM SiGe HBTs for a switching pair, shows more distortion in output waveform (Figure 2.4.5 (a)) than RX4 with an IM SiGe HBT switching pair (Figure 2.4.5 (b)) in terms of transient peaks and durations [65]. From this experiment, we can conclude that 1) since mixers are the last stage in a receive chain, the impact of laser beam strikes is critical in the overall receiver operation, 2) the distortion in envelope signal (or the degradation in SNR), which contains IF data in communications systems, can be significant when the IF band becomes higher, and 3) IM SiGe HBT switching pairs are effective in reducing not only transient peaks but also transient durations.

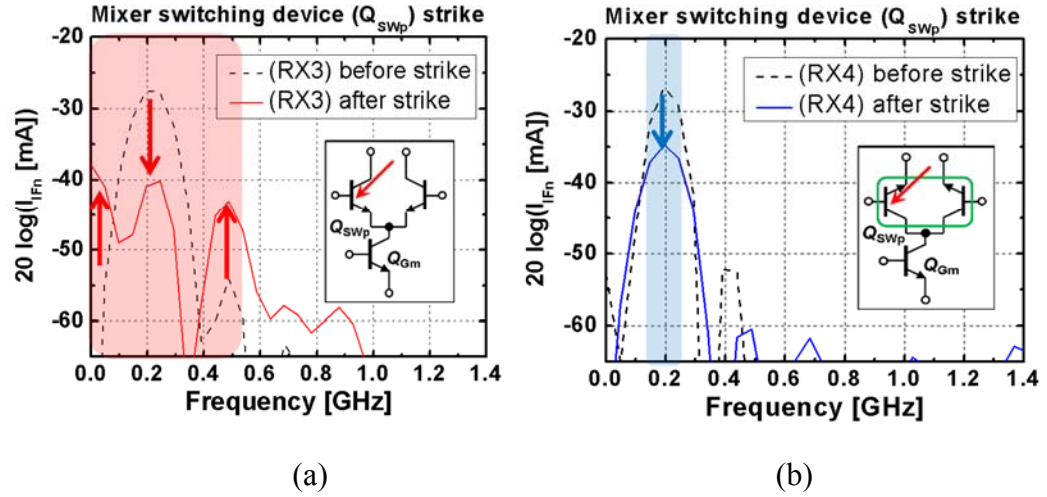


Fig. 6. Frequency spectrum before/after the laser beam strikes the switching-pair transistors (Q_{swp}) of mixers in (a) RX3 and (b) RX4. The outputs were measured at the mixer output port IF_n .

The frequency spur induced by SETs is shown in Figure 2.4.6. By applying the fast Fourier transform to the time domain waveform in Figure 2.4.5, the impact of SETs in the frequency domain can be analyzed. When the laser beam strikes a switching transistor Q_{SWP} , both RX3 and RX4 exhibit a reduction of the IF signal at 0.2 GHz due to the interruptions shown in Figure 2.4.5. For RX3, which uses FM SiGe HBTs for the switching pair, the reduction of the IF signal is larger than RX4, with an IM SiGe HBT switching pair, by 5.5 dB. In addition to the IF spurs, the SETs in RX3 cause noise at adjacent frequencies at DC and 0.5 GHz (Figure 2.4.6 (a)). These distortions inevitably degrade SNR of receivers and may lead to data corruption. On the other hand, RX4 shows major degradation in the IF signal. For other frequencies, the interruption associated with SETs is not significant (Figure 2.4.6. (b)).

Considering the findings in this work, the use of IM SiGe HBTs is effective in reducing the impact of SETs. The IM SiGe HBT-based switches and LNAs exhibit reduced transient peaks, while the IM SiGe HBT-based down-conversion mixer shows a reduction in both transient peaks and durations. In order to fully exploit IM SiGe HBTs as an RHBD approach, the degradation of RF performance should be compensated by additional device, circuit, or system level techniques.

2.4.4 Summary

Various receivers with SET-mitigated RF circuit blocks are designed for the investigation of IM SiGe HBTs' functional effects on receiver operation. In general, IM SiGe HBTs help reducing transient peaks and durations, but the effect of each SiGe HBT in a receiver output is different. IM SiGe HBTs in RF switches and LNAs are effective in

the reduction of transient peaks, while IM SiGe HBTs in mixers mitigate both peaks and durations. Depending on the requirements of RF performance, the use of IM SiGe HBTs can be a viable RHBD technique for space-based RF applications.

CHAPTER 3. IMPACT OF TECHNOLOGY SCALING ON RHBD

3.1 Introduction

It is well known that inverse-mode (IM) silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) are less susceptible to single-event transients (SETs) compared to forward-mode (FM) SiGe HBTs [1], [19], [20], [66]. Specifically, IM SiGe HBTs exhibit smaller transient peaks and shorter durations than FM SiGe HBTs, which is fundamentally attributed to: 1) the better isolation of the physical emitter terminal from the substrate-subcollector transient tail currents, and 2) higher internal electric field between the base and the physical emitter terminals [20], [66]. These benefits are crucial for applications operating under radiation-intense conditions, reducing potential loss of data in real-time systems and degradation in device reliability and circuit performance [4], [5], [67]. When it comes to the damage associated with total ionizing dose (TID), IM SiGe HBTs show good tolerance against TID [68]-[71], since their performance does not heavily rely on the quality of oxide layers, as it does, for instance, with CMOS transistors [67], [72]-[74]. With these benefits of reduced SET sensitivity and TID damage, there has been much effort in the literature to utilize IM SiGe HBTs in various types of digital circuits [20], [66], [75], and analog blocks such as current mirrors [16] and bandgap references [22], and radio frequency (RF) building blocks [23], [64], [65].

While IM SiGe HBTs have shown promising SET-mitigation results for space-based applications, there are some disadvantages associated with using them, which can impose limitations on the general applicability of IM SiGe HBTs. Unlike the mitigation strategies for CMOS transistors, which do not necessarily degrade device/circuit performance [76]-

[79], the IM SiGe HBTs inevitably exhibit decreased current gain (β) [50] and degraded high frequency performance metrics, including unity gain cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}), due to an unfavorable germanium profile and larger parasitics. Thus, in the literature IM SiGe HBTs have been mainly applied to non-critical transistors such as biasing circuitry [21], [22], passive circuits [64], or buffer stages [23], where the limited performance of IM SiGe HBTs can be negligible in circuit operation or does not directly affect the overall circuit/system performance. However, if an IM SiGe HBT is used in an active gain stage of an RF low-noise amplifier (LNA), for example, it can significantly degrade gain or noise performance. Hence, in spite of the potential SET mitigation offered, it would not be a preferable choice due to the severe performance degradation. This tradeoff associated with IM SiGe HBTs is originated from the inherent asymmetries in the device structure.

Fortunately, aggressive scaling down of a SiGe HBT technology has significantly improved the RF performance of IM SiGe HBTs (as well as FM ones), extending the peak f_T of IM SiGe HBTs beyond several tens of GHz [24]. This implies that the IM SiGe HBTs can potentially be utilized as active gain stages for space-relevant low-GHz RF circuits without substantial performance loss. One of the key building blocks for RF transceivers is an LNA. As the first stage in a typical receive chain, an LNA should provide enough gain, low noise figure, and high linearity with low power consumption and compact chip size [80]. In the design of an RF LNA, an IM SiGe HBT in an active gain stage needs to provide reasonable power gain and good noise figure for proper RF receiver operation. Thus, by utilizing IM SiGe HBTs, the resulting circuits should then have decent RF performance with much less susceptibility to single-event transients.

To date, however, few studies in the literature have addressed the potential capability of IM SiGe HBTs as active gain stages for RF circuits. In the present work, an RF (2.4 GHz) LNA is selected to characterize the impact of IM SiGe HBTs on RF circuit performance and investigate the achievable SET mitigation as a viable radiation-hardening-by-design (RHBD) approach. The IM-SiGe-HBT-based LNA designed using an advanced 90 nm SiGe BiCMOS platform (GlobalFoundries SiGe 9HP) shows acceptable RF performance and exhibits substantial reduction in SETs compared to recent work [23]. In order to characterize transient waveforms, a through-wafer, two-photon absorption (TPA) pulse-laser technique is used. Section 3.2 will describe the design of an LNA with IM SiGe HBTs and show the RF performance of the LNAs. Details of the experimental set-up and SET results are discussed in Section 3.3. Section 3.4 will summarize the findings of this investigation.

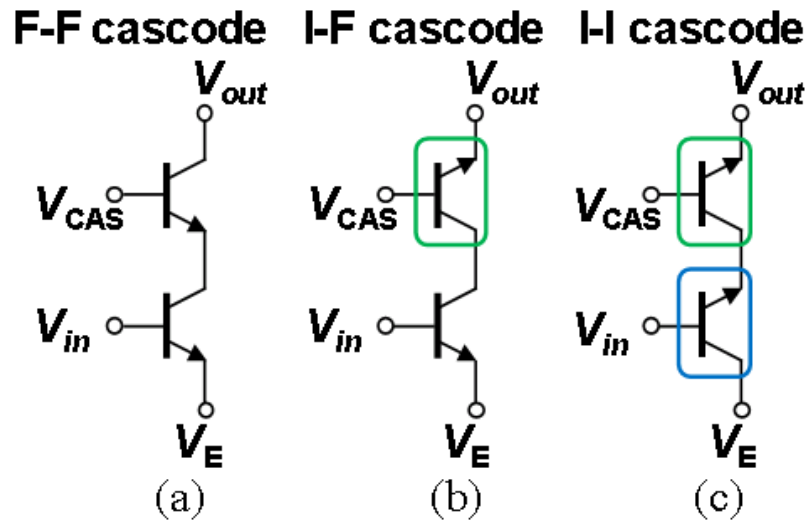


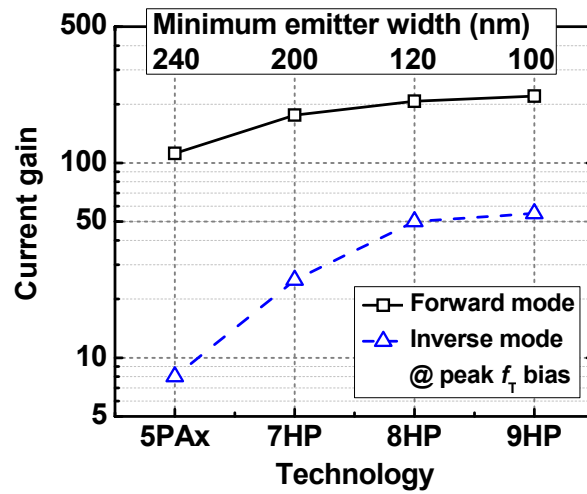
Figure 3.1 - Cascode configurations: (a) the conventional FM SiGe HBTs, (b) a hybrid type (an IM SiGe HBT for the common-base stage), (c) the proposed full-IM-SiGe-HBT cascode structures.

3.2 LNA Design with Inverse-Mode SiGe HBTs

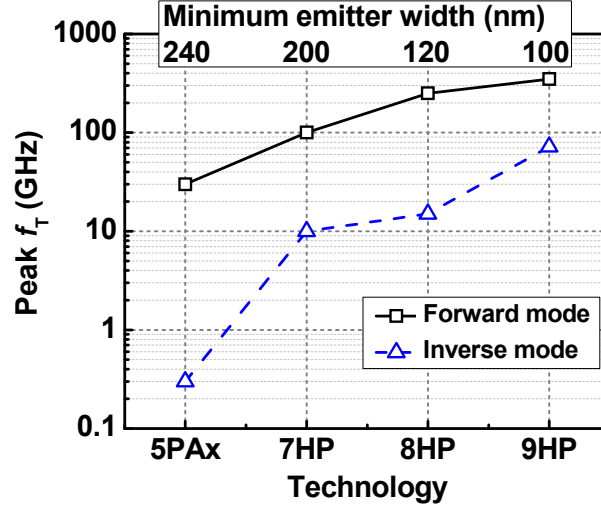
A common amplifying core of an RF LNA is a cascode configuration as shown in Figure 3.1. The bottom common-emitter (CE) transistor amplifies and translates the input voltage into the collector current, and then in the top common-base (CB) transistor the amplified current injected from the emitter flows out of the collector terminal with unity current gain [81]. The collector current of the CB transistor multiplied by the load impedance will be transformed back into the (amplified) output voltage. In a conventional RF LNA, a cascode configuration of two FM SiGe HBTs (F-F cascode, Figure 3.1 (a)) is used for the best LNA performance, while in the recently proposed SET-mitigated LNA, a hybrid-type cascode (I-F cascode, Figure 3.1 (b)), in which an IM SiGe HBT was applied for the CB transistor was used [23]. This type of cascode provides reduced transients with the minimal LNA performance degradation, in spite of the relatively low f_T and high minimum noise figure (NF_{min}) associated with the IM SiGe HBT. This is because 1) the transconductance (g_m) of the CE transistor determines the overall LNA gain and noise figure (NF), and 2) the CB transistor mainly acts as a current buffer [53].

In an advanced SiGe HBT technology such as a 90 nm SiGe BiCMOS platform, it becomes possible to use IM SiGe HBTs for active gain stages (I-I cascode), as shown in Figure 3.1 (c), since technology scaling has improved the RF performance of IM SiGe HBTs significantly. The simulated current gain, peak f_T , and NF_{min} of both FM and IM SiGe HBTs across technology generations are presented in Fig. 2. The simulation data were obtained by using relevant process design kits for each generation. The technology names of 5PAx, 7HP, 8HP, and 9HP represent 350 nm, 250 nm, 130 nm and 90 nm scaling nodes, respectively, and the drawn emitter width is somewhat different from the node numbers

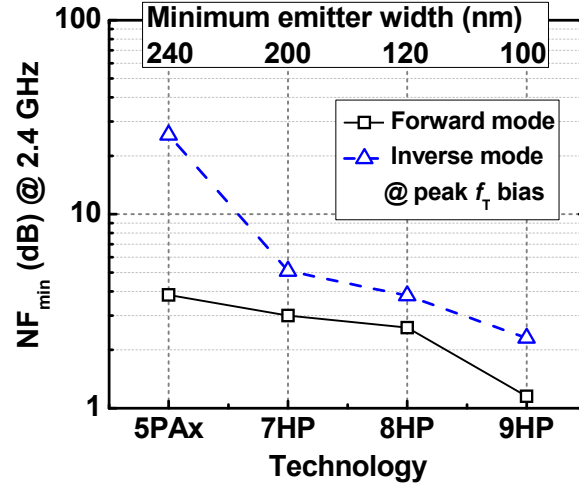
due to fabrication issues. As shown in Figure 3.2 (a) and (b), both the current gain and the peak f_T have improved significantly over the generations. While the DC current gain of 9HP IM SiGe HBTs is lower than the 5PAx FM ones, the 9HP IM SiGe HBTs' peak f_T is higher than the 5PAx FM ones due to reduced parasitics from lateral scaling. In Figure 3.2 (c), the NF_{min} of the 9HP IM SiGe HBTs is comparable to the FM NF_{min} of other technologies, implying that 9HP IM SiGe HBTs can provide low NF for RF LNAs when they are used in the active gain stages. However, when it comes to SET sensitivity, it should be noted that the intrinsic device volume in advanced SiGe HBTs is more susceptible to SETs than the SiGe HBTs in the earlier generations [82]. This is mainly attributed to increased Ge contents in the base region, which lead to 1) larger transient peak from the increased current gain and 2) greater charge separation due to Ge-induced electric field [82]. Therefore, the use of IM SiGe HBTs can potentially compensate the increased SET sensitivity associated with the advanced SiGe HBTs.



(a) (continued)



(b)



(c)

Figure 3.2 - (a) Simulated current gain of both FM and IM SiGe HBTs under the peak f_T bias for different SiGe technology generations. (b) Simulated peak f_T for both FM and IM SiGe HBTs. (c) Simulated NF_{min} at 2.4 GHz under the peak f_T bias. All devices have a common emitter length of 10 μm .

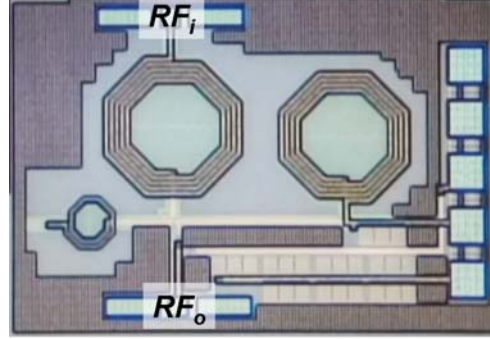
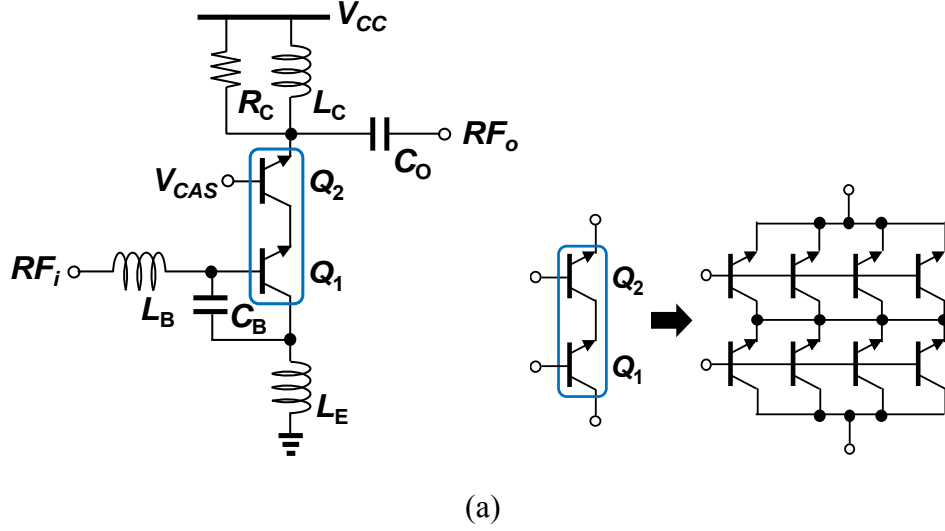
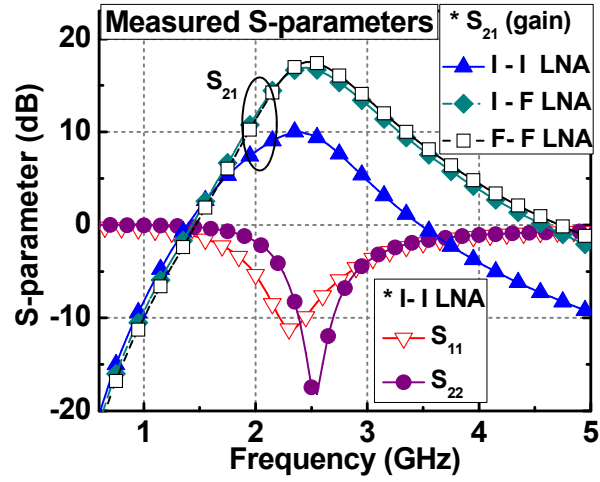


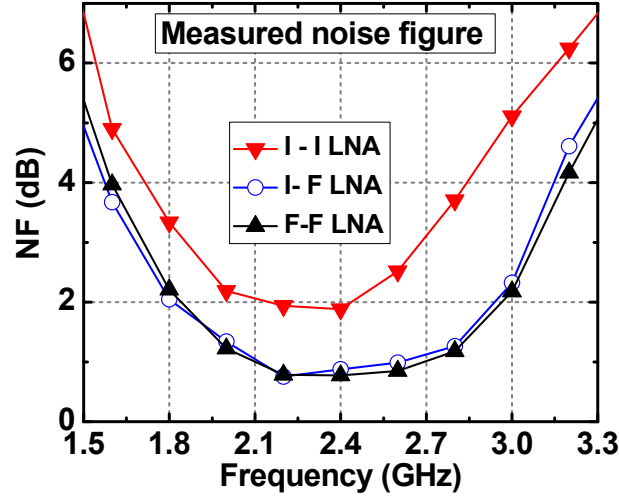
Figure 3.3. (a) Schematic of the proposed LNA (I-I cascode) with a full IM SiGe HBTs (top) and the actual configuration of the cascode stage (bottom). Biasing is not shown. (b) A chip micrograph of the fabricated LNA. The total chip size is about 1.22 mm^2 ($1.35 \text{ mm} \times 0.90 \text{ mm}$).

The schematic of the I-I cascode LNA is shown in Figure 3.3 (a). Each of the CE (Q_1) and the CB (Q_2) transistors in the cascode stage is composed of four parallel-connected SiGe HBTs for the optimization of noise figure and impedance matching. The total emitter area of Q_1 (or Q_2) is $4 \times 2.0 \times 0.1 \text{ } \mu\text{m}^2$. The degenerated emitter inductor (L_E) provides negative feedback for stability, and presents real impedance to the base of Q_1 [55]. The base inductor L_B and the base-emitter capacitor C_{BE} are tuned for input impedance

matching and noise figure optimization. The collector inductor L_C and the output capacitor C_o are used for output impedance matching. In addition, the collector resistor R_C is inserted to broaden the output matching characteristics. The prototype LNA was designed for 2.4 GHz general-purpose space applications and fabricated using the GlobalFoundries 90 nm 9HP SiGe BiCMOS platform. The chip micrograph is shown in Figure 3.3 (b) and the die size is $1.35 \times 0.90 \text{ mm}^2$. The total of three LNAs using different cascode structures (as shown in Figure 3.1) were designed to compare their relative RF performance and SET sensitivity.



(a) (continued)



(b)

Figure 3.4 - (a) Measured S-parameters of the proposed I-I cascode LNA. For gain comparison, the S_{21} of the I-F and the F-F cascode LNAs are shown. (b) Measured NF of the three LNAs.

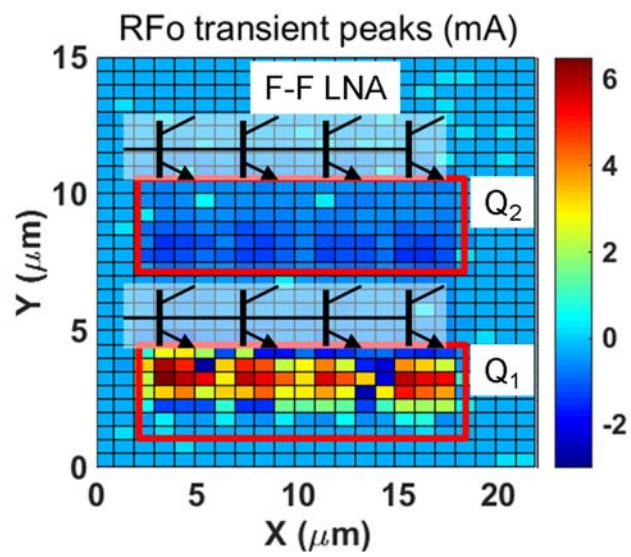
The measured S-parameters and noise figure of the three LNAs are presented in Figure 3.4 (a) and (b), respectively. The LNAs were characterized with on-wafer measurements using a two-port network analyzer (Agilent PNA E8361C). For the noise-figure measurement, a signal analyzer (Agilent PXA N9030A) and a noise source (Agilent N4002A) were used. In Figure 3.4 (a), the input and the output impedance of the I-I cascode LNA are matched around 2.4 GHz. The peak gain (S_{21}) is 10 dB, which is about 7 dB lower than the F-F and the I-F cascode LNAs as expected from Figure 3.2 (b). The measured NF of the three LNAs is shown in Figure 3.4 (b). At 2.4 GHz, the I-I cascode LNA exhibits the NF of 1.9 dB, while the other two LNAs have about 1.3-dB lower NF. While the I-I cascode LNA has degraded gain and NF, the absolute numbers of 10-dB gain and 1.9-dB NF are promising results for RF LNAs, considering the use of the IM SiGe HBT as an active gain stage for a CE transistor.

Table 3.1 - RF LNA Performance Summary

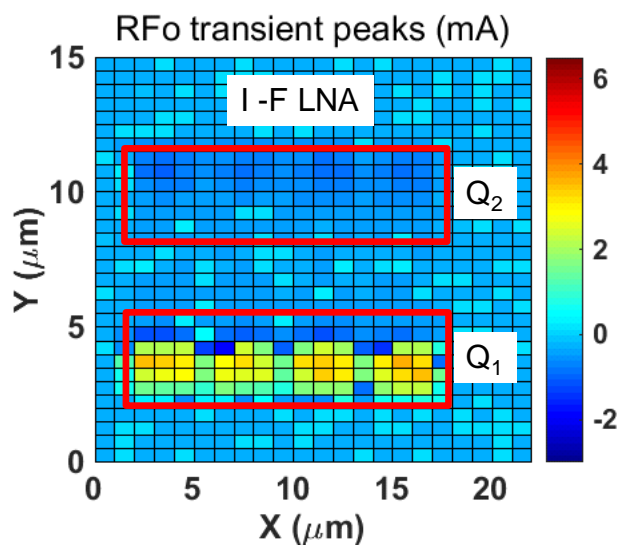
Performance parameter	F-F cascode LNA	I-F cascode LNA	I-I cascode LNA	F-F cascode LNA*
Technology	9HP (90 nm)	9HP (90 nm)	9HP (90 nm)	8HP (130 nm)
Frequency [GHz]	2.4	2.4	2.4	2.4
S_{21} [dB]	17.3	16.8	10.0	14.3
Noise figure [dB]	0.8	0.9	1.9	1.5
Input P1dB [dBm]	-23	-21	-14	-18
Input IP3 [dBm]	-13.8	-13.4	-9.4	-8.5
P_{DC} (core) [mW] ($V_{CC} \times I_{DC}$)	2.6 (2.5x1.04)	2.3 (2.5x0.92)	2.0 (2.5x0.81)	2.6 (2.5x1.04)

* Simulation results

The performance of the F-F, the I-F, and the I-I cascode LNAs is summarized in Table 3.1. For comparison, the simulated 130 nm (8HP) F-F LNA results are added. The I-I cascode LNA has degraded S_{21} and NF, while it exhibits better linearity such as the input 1-dB compression point (P1dB) and the input third-order intercept point (IP3) than the F-F and the I-F cascode 9HP LNAs. The performance gap between the I-I cascode 9HP LNA and the F-F cascode 8HP LNA is much smaller due to the benefits of technology scaling.



(a)



(b) (continued)

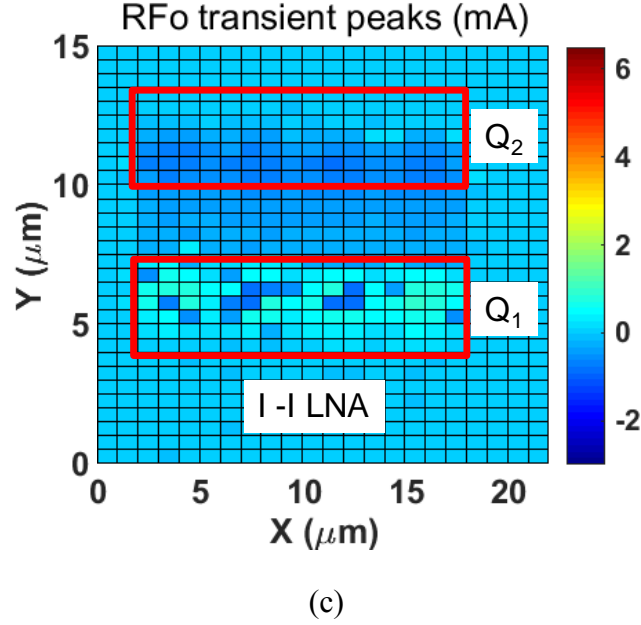


Figure 3.5 – Two-dimensional raster scan images for (a) the F-F cascode, (b) the I-F cascode, and (c) the I-I cascode LNAs. The scanned area includes both Q_1 and Q_2 transistor region. Since each of Q_1 and Q_2 is composed of four parallel-connected transistors, as shown in Figure 5 (a), some repeating patterns are observed.

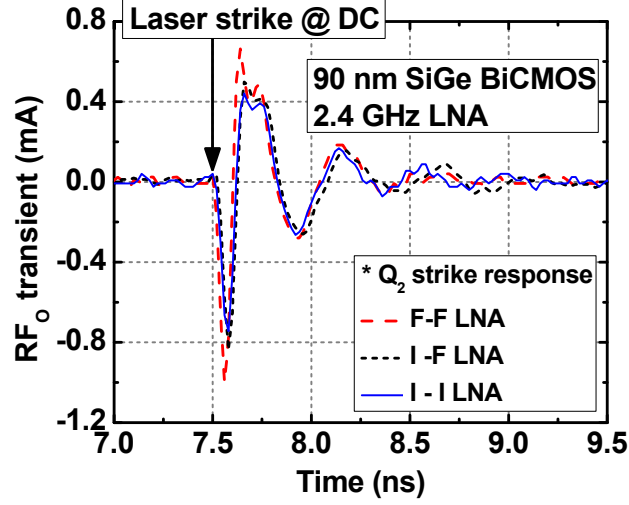
3.3 Pulsed-Laser Experiment Results and Discussion

A through-wafer TPA pulse-laser experiment [47], [48] was conducted at the US Naval Research Laboratory (NRL) for measuring the resultant transient waveforms for each LNA. The generated laser beam had a pulse duration of 150 fs, a wavelength of 1.26 μm , and full width at half maximum (FWHM) spot size of 1.2 μm . The LNA chips were attached to custom-designed high-speed printed circuit boards (PCBs) and wire-bonded for DC bias and RF signals. In order to fully capture high-frequency transients, a high-speed oscilloscope (Tektronix DPO 71254) was connected to the signal lines through bias tees. For the LNA operation, we applied a 2.5 V power supply to both V_{CC} and V_{CAS} terminals, while the cascode branch current is maintained at about 0.9 mA via current source biasing

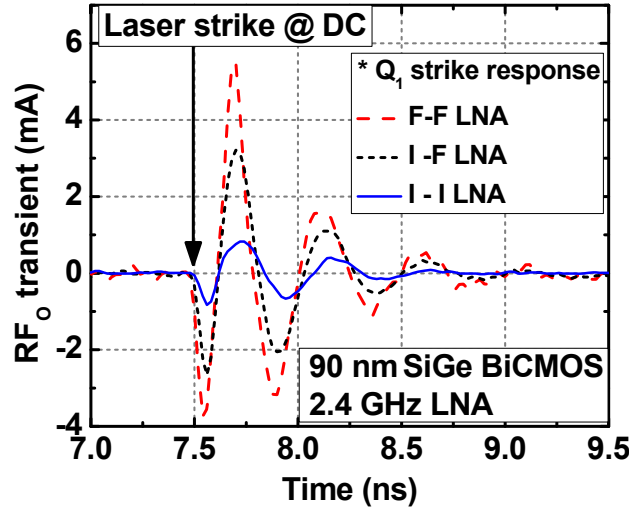
(see Table 3.1). The fixed laser energy of 35.6 pJ was used throughout the experiment. Since the relationship between the laser energy and the heavy-ion LET is nonlinear, and dependent on the specific technology, it is difficult to directly match equivalent LET [59]-[62]. However, it is expected that the LET lies between 10 and 100 MeV·cm²/mg [59]-[61].

Two-dimensional (2-D) raster scan images of the F-F, the I-F, and the I-I cascode LNAs are shown in Figure 3.5. The cells with high intensity denote larger single-event transient peaks while the cells with low intensity mean smaller peaks. In addition, depending on the polarity of the transient peak, the 2-D raster scans show either blue or red colors. Since in the LNA design, four SiGe HBTs were connected in parallel for the optimized circuit performance, both the CE transistor (Q_1) and the CB transistor (Q_2) show the 4X horizontally repeating patterns in the raster scans.

For all three LNA cases, the CE transistor (Q_1) strike shows larger transient peaks compared to the CB transistor (Q_2) strike. This is because when Q_1 is struck the total branch bias current changes dynamically. On the other hand, when Q_2 is struck, the bias current still tries to stay constant against the perturbations (i.e., SETs) due to the negative feedback effect associated with Q_1 , generating smaller transient peaks. Compared with the F-F (Figure 3.5 (a)) and the I-F (Figure 3.5 (b)) cascode LNAs, the I-F cascode has reduced peaks for the Q_2 strike due to the use of an IM SiGe HBT, while the peaks from the Q_1 strike are similar for both cases. The I-I cascode LNA (Figure 3.5 (c)) exhibits the further reduced transient peaks for the Q_1 strike, implying less change in the branch bias current.



(a)



(b)

Figure 3.6 - Output time-domain transient waveforms under DC states for (a) Q_2 strike and (b) Q_1 strike cases. The waveforms are measured on the most sensitive points found along the X, Y, and Z axes.

The time-domain transient waveforms under DC conditions are shown in Figure 3.6. The most sensitive points along the X, Y, and Z axes were found with the laser focus and measured for each transistor. As expected from Figure 3.5, the F-F cascode LNA shows

the largest peaks for both the Q_2 and the Q_1 strike cases. For the Q_1 strike, the peak reduction of the I-I cascode LNA is about 81% and 69% when compared to the F-F and the I-F cascode LNAs, respectively. With regard to the durations, all three LNAs exhibit a similar transient duration of about 1.5 ns. In addition, since both the input and the output of the LNAs are matched to 2.4 GHz, the output transient is different from the response directly from the cascode collector terminal. Instead, the transient waveform can be viewed as a band-pass-filtered response.

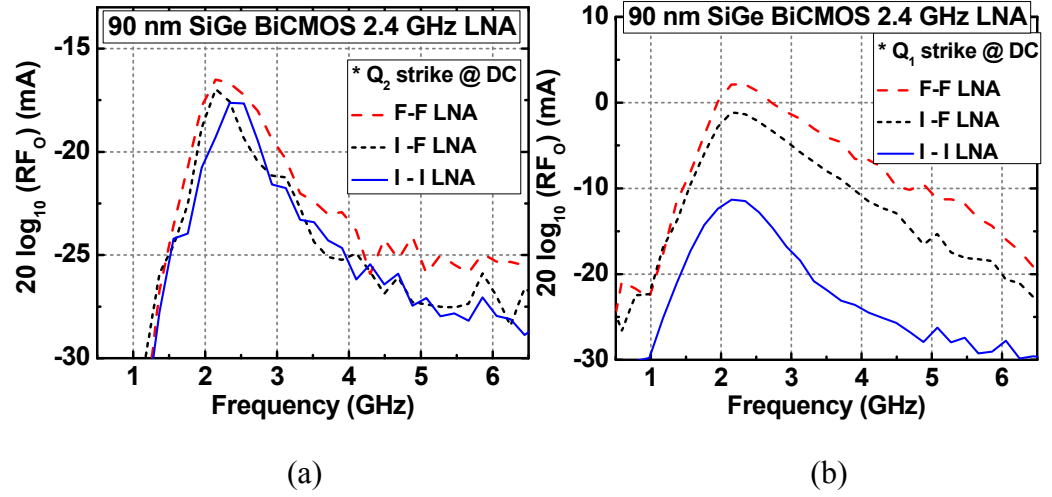
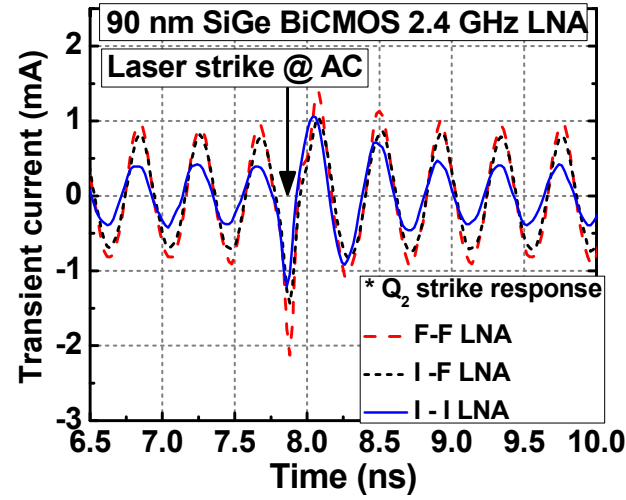


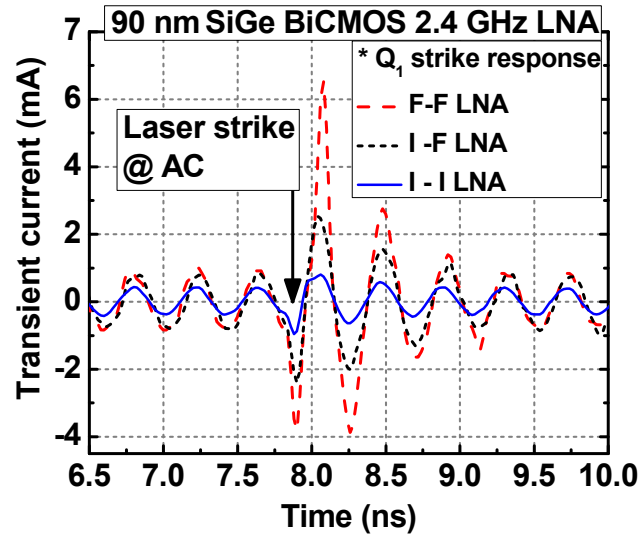
Figure 3.7 - Frequency spectrum of the F-F, the I-F, and the I-I cascode LNAs under DC bias condition. (a) Frequency spur when the laser strikes Q_2 . (b) Frequency spur when the laser strikes Q_1 .

By applying the fast Fourier transform (FFT), the frequency-domain response of the time-domain waveform is obtained, and the results are presented in Figure 3.7. Because the LNAs are in a DC bias state, the power spectral density (PSD) at each frequency should be ideally negative infinity. When the laser strikes the active transistor region, the corresponding PSD appears in the frequency spectrum. As mentioned above, the peak PSD

is observed at the matched frequency of 2.4 GHz due to the filtering effects. For the Q_2 strike (Figure 3.7 (a)), the F-F cascode LNA has about a 1.2-dB larger peak than the I-I cascode LNA. On the other hand, for the Q_1 strike (Figure 3.7 (b)), the difference between two LNAs is about 13 dB at 2.4 GHz.

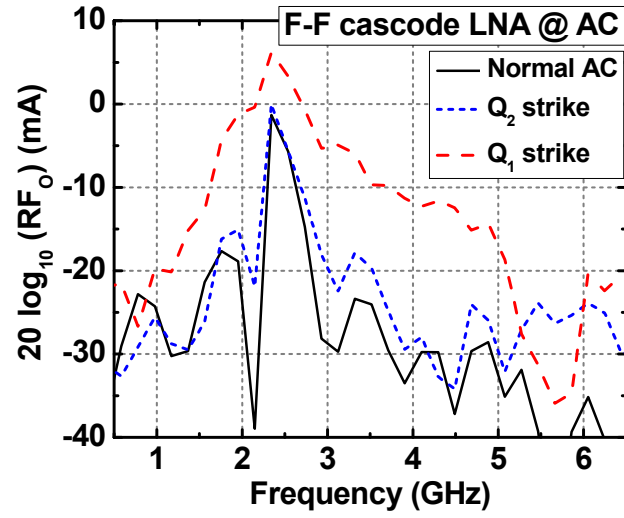


(a) (continued)

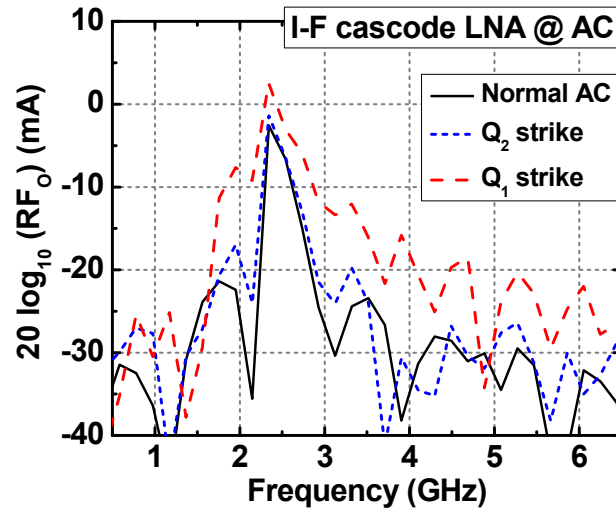


(b)

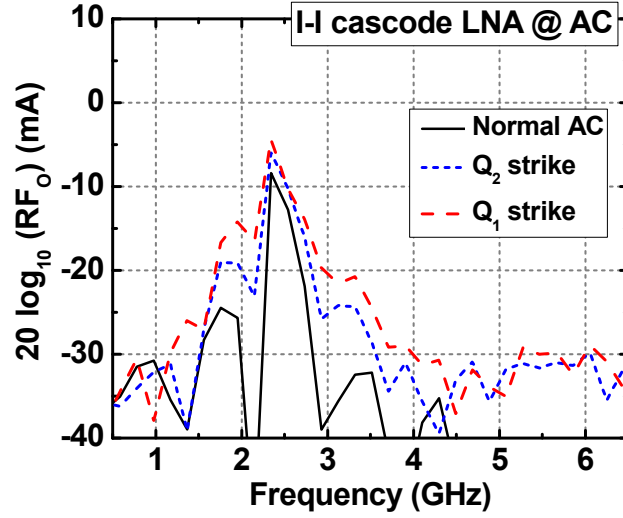
Figure 3.8. Output time-domain transient waveforms with RF input signals for (a) Q_2 strike and (b) Q_1 strike cases. The RF signals have the AC power of -30 dBm and a frequency of 2.4 GHz. The waveforms are measured on the most sensitive points found along the X, Y, and Z axes.



(a)



(b) (continued)



(c)

Figure 3.9 - Frequency spectrum under normal AC operation and under the laser strike for (a) the F-F cascode LNA, (b) the I-F cascode LNA, and (c) the I-I cascode LNA.

The time-domain transients with an RF input signal are shown in Figure 3.8. The input signal has an AC power of -30 dBm with a single-tone frequency of 2.4 GHz. Since the power gain of the F-F cascode LNA is the highest, it shows the largest current swing, as opposed to the I-I cascode LNA, which has the smallest output current swing. For the Q_2 strike cases (Figure 3.8 (a)), all three LNAs have similar transient duration of about 1.0 ns, which is slightly shorter than the DC response shown in Figure 3.6. The faster transient recovery can be attributed to more frequent charge flows depending on the phase of the input signal. The Q_1 strike results are shown in Figure 3.8 (b). Compared to the Q_2 strike case, the settling time of the F-F and the I-F cascode is longer possibly due to higher transient peaks. The I-I cascode LNA exhibited about 85% and 52% reduction in transient peaks compared to the F-F and the I-F cascode LNAs. This can be an additional benefit of

using the I-I LNA in terms of long term device/circuit reliability, since the voltage or current spikes during heavy-ion spikes can impose electrical stress on the transistors.

In Figure 3.9, the frequency spectrum under normal AC operation is shown when the transistors are struck by the laser. Since the LNAs are driven with a single-tone RF input signal, the ideal output frequency spectrum should contain the PSD at the same frequency. However, due to the nonlinearity associated with the transistors and the limited sampling rate of the oscilloscope, other frequency components are observed as well. When the laser strikes Q_2 , the change in the frequency spectrum is not significant compared to the normal operation response for all three LNAs. However, for the F-F cascode LNA (Figure 3.9 (a)), the frequency spur becomes dominant over the normal response when the laser strikes Q_1 . The PSD of the fundamental frequency increases by 8 dB and the broadband noise components occur from 1 to 5 GHz. For the I-F cascode LNA (Figure 3.9 (b)), the interference from the Q_2 strike is less significant than the F-F cascode LNA case. The I-I cascode LNA exhibits further minimized perturbation in the frequency spectrum (Figure 3.9 (c)). The peak PSD increases by only 4 dB and the broadband noise components are much less dominant compared with other LNAs.

In summary, the I-I cascode LNA shows the minimum susceptibility to single-event transients, which is verified and analyzed in both time and frequency domains. In addition, since the I-I cascode LNA exhibits good RF performance, exploiting the benefits of technology scaling, the use of IM SiGe HBTs as active gain stages can be a viable, practical RHBD approach for space-based applications.

3.4 Summary

The use of inverse-mode (IM) SiGe HBTs as active gain stages in RF LNA design is investigated for SET mitigation. Conventionally, despite their SET-mitigation capability, IM SiGe HBTs are not suitable for active gain stages due to severe performance degradation. With the benefits of aggressive technology scaling, however, the RF performance of IM SiGe HBTs has been significantly improved, thereby enabling them to be utilized in active gain stages with decent RF performance. The cascode with inverse-mode common-emitter and common-base SiGe HBTs is used for LNA design and the LNA achieves enough RF gain and low noise figure. With regard to SET mitigation, the proposed IM-SiGe-HBT-based LNA exhibits roughly an 85% reduction in transient peaks compared to the conventional FM-based LNA.

CHAPTER 4. CRYOGENIC OPERATION OF SIGE LNAS

4.1 Introduction

Extreme environment applications typically impose severe operation constraints to their constituent devices and circuits as opposed to commercial electronics [83]. For example, the circuits for space-based applications should provide reliable performance under tough operation conditions such as wide temperature range and radiation-intense environment. Recently, researchers have started to exploit inverse-mode (IM) SiGe HBTs, in which designers intentionally swap the connection of the collector and the emitter in a conventional forward-mode SiGe HBT, for the mitigation of SETs in various circuits [21], [64], [75]. In spite of the reduced sensitivity to transients, the performance of the inverse-mode-based circuits need to be characterized for a wide range of temperature including a cryogenic condition in order to assess their practicality in extreme environment applications such as space-based systems. However, most studies have focused on the cryogenic operations of the forward-mode-based SiGe HBT circuits [25]-[26].

In this paper, we present cryogenic characterization results of inverse-mode-based SiGe HBT circuits for the investigation of any potential issues associated with the use of inverse mode. As a representative device-under-test (DUT), a radio-frequency (RF) low-noise amplifier (LNA) is chosen. The prototype LNA used in this work has been proposed for SET mitigation, exhibiting minimal performance degradation such as gain or noise figure when it is compared to the conventional forward-mode SiGe HBT LNA [23].

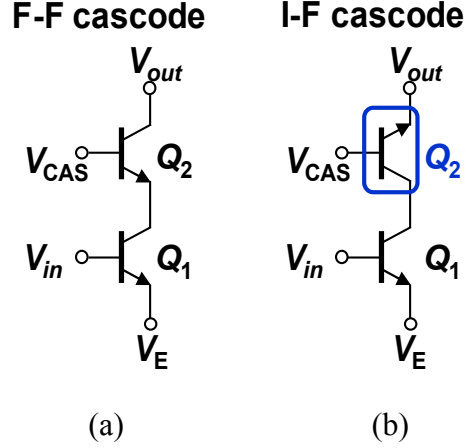


Figure 4.1 - (a) Conventional forward-mode-only SiGe HBT cascode (F-F cascode) configuration (b) the cascode configuration with an inverse-mode common-base (CB) SiGe HBT (I-F cascode) for the mitigation of single-event transients [23].

4.2 Design of a SiGe LNA with Inverse-Mode HBTs

In a typical RF LNA design, the cascode structure has been widely used as an amplifier core, whose schematic is shown in Figure 4.1 (a) [55]. With regard to the mitigation of single-event transients, the modified cascode structure termed I-F cascode, in which an inverse-mode SiGe HBT is used in the place of the CB stage as shown in Fig. 1 (b), has been suggested in [23]. Because the inverse-mode SiGe HBT exhibits acceptable RF performance for low-GHz operation, minimal degradation is expected compared to the conventional forward-mode-only design termed F-F cascode in Figure 4.1 (a). Therefore, the resultant advantage of the I-F cascode LNA is the significantly reduced susceptibility to single-event transients [23].

The LNAs were fabricated using the GlobalFoundries 130 nm SiGe BiCMOS (8HP) technology, which features the peak f_T/f_{MAX} of 220/250 GHz [45]. The SiGe HBTs used in the LNAs have the same (physical) emitter area of 120 nm x 2.5 μ m for both forward and

inverse mode operation. The total chip size is 1.5 mm^2 ($1.0 \text{ mm} \times 1.5 \text{ mm}$), including measurement pads. In order to compare the RF performance of the I-F cascode LNA (Figure 4.1 (b)) with a conventional forward-mode-only SiGe HBT LNA, an additional reference LNA (Figure 4.1 (a)) was designed and characterized as well.

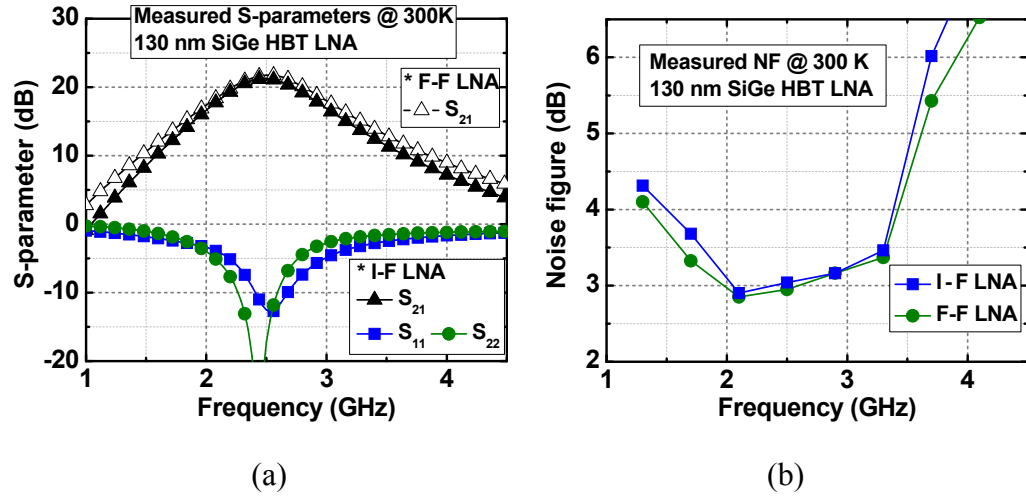


Figure 4.2 - (a) Measured S-parameters of the I-F cascode LNA. For gain comparison, the measured S₂₁ of the conventional F-F cascode LNA is shown. (b) Measured noise figure of both the I-F and the F-F cascode LNAs.

4.3 Cryogenic Characterization

For cryogenic characterization, liquid nitrogen was used as a cryogen to cool the ambient temperature down to 78 K. The LNAs were measured in a custom-designed open-cycle probe station. The liquid nitrogen in the dewar flows into the backside of the chuck with the high pressure provided from the compressed nitrogen gas, while in the inside the chamber, a vacuum condition is maintained by an external pump. For the LNA

measurement, a two-port network analyzer (Agilent PNA E8361C), analog signal generators (Agilent PSG E8257), a spectrum analyzer (E4407B), and a noise source (Agilent N4002A) were selectively used for S-parameter, linearity, and noise figure. All measurement data were obtained from on-wafer probing.

The measured RF performance of the LNAs at room temperature (300 K) is presented in Figure 4.2. In Figure 4.2 (a), the measured S-parameters of the I-F cascode LNA is shown. While the peak S_{21} of both the I-F and the F-F cascode LNAs are similar about 21 dB, the latter has the slight higher (~ 0.5 dB) peak than the former. In addition, it is observed that the I-F cascode LNA has steeper roll-off slope from the peak along the frequency than the F-F cascode LNA. The measured noise figure (NF) of both the LNAs at 300 K are shown in Figure 4.2 (b). At the center frequency, the I-F cascode LNA has about 0.1 dB higher NF than the F-F cascode LNA, whereas the NF increase in the I-F cascode LNA becomes larger in the lower (< 2 GHz) or the higher (> 3 GHz) frequency region. Overall, the gain and the noise performance of the I-F cascode LNA is similar to the conventional F-F cascode LNA. Thus, when the inverse-mode SiGe HBT is used as a current buffer stage in the place of Q_2 (Figure 4.1 (b)), the performance degradation associated with the use of the inverse-mode is can be negligible for operation at room temperature.

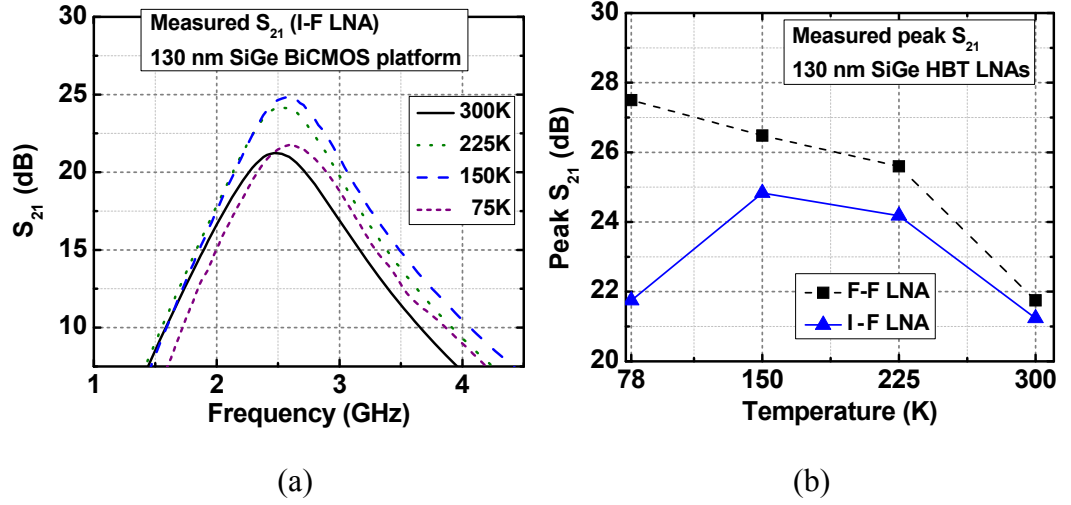


Figure 4.3 - (a) Measured gain (S_{21}) of the I-F cascode LNA versus frequency at different temperatures. (b) Measured peak S_{21} of both the I-F and F-F cascode LNAs versus temperature.

The measured gain (S_{21}) response at different temperatures is shown in Figure 4.3. In Figure 4.3 (a), the S_{21} of the I-F cascode LNA is presented versus frequency for 300 K, 225 K, 150 K, and 78 K. The frequency shift across temperature is not significant while the variation in the peak values is more dominant. The gain of the I-F cascode LNA increases from 21.3 dB to 24.8 dB until the temperature reaches 150 K. However, when the temperature is at 78 K, the peak gain drops to 21.6 dB. This gain reduction is an opposite result from the previous studies for cryogenic operation of forward-mode SiGe HBTs [84], [87], which exhibit monotonic increase of f_T/f_{MAX} down to 4.5 K [84]. Thus, the gain drop is attributed to the performance degradation associated with the use of the inverse-mode at cryogenic temperature. For comparison, the peak gain of both the I-F and the F-F cascode LNAs is shown in Figure 4.3 (b). As expected, the F-F cascode LNA exhibits monotonic gain increase from 21.8 dB to 27.5 dB as temperature decreases.

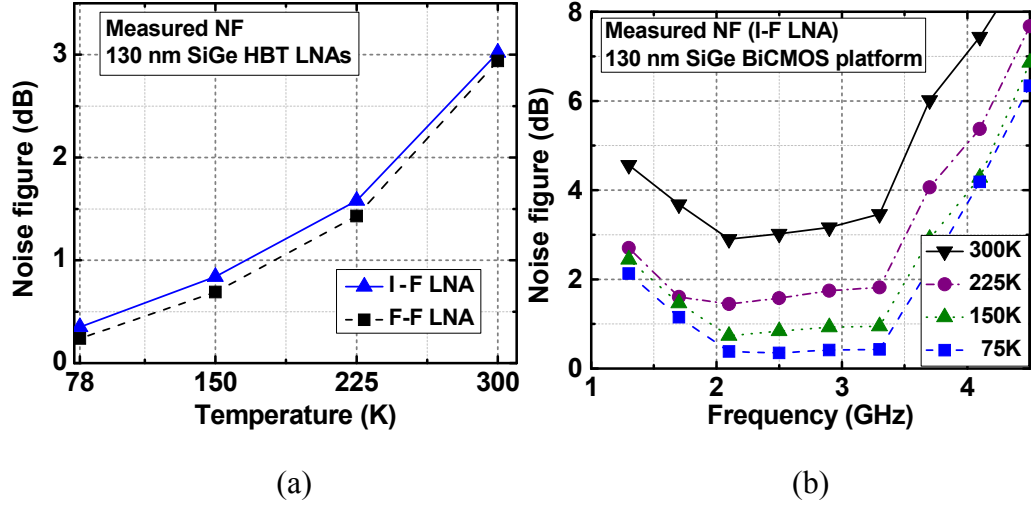


Figure 4.4 - (a) Measured noise figure of the I-F cascode LNA at different temperature versus frequency. (b) Comparison of NF between the I-F and the F-F cascode LNAs across temperature.

The measured noise figure of the I-F cascode LNA at different temperatures is presented in Figure 4.4. In addition, the results were reproducible among the samples. Unlike the peak gain response in Figure 4.3, when the temperature cools down to 78 K, the NF of the I-F cascode monotonically decreases (Figure 4.4 (a)), since the noise generation in active devices directly depends on the ambient temperature [49]. Frequency shift across temperature is not significant and the overall response shape is maintained except for the NF values. The measured NFs of both the I-F and the F-F cascode LNAs at the operation frequency versus temperature are shown in Figure 4.4 (b). The NF of the I-F cascode LNA at the operation frequency falls from 3.0 to 0.3 dB. Across temperature, the I-F LNA has slightly higher NF (0.1~0.2 dB) than the F-F cascode LNA.

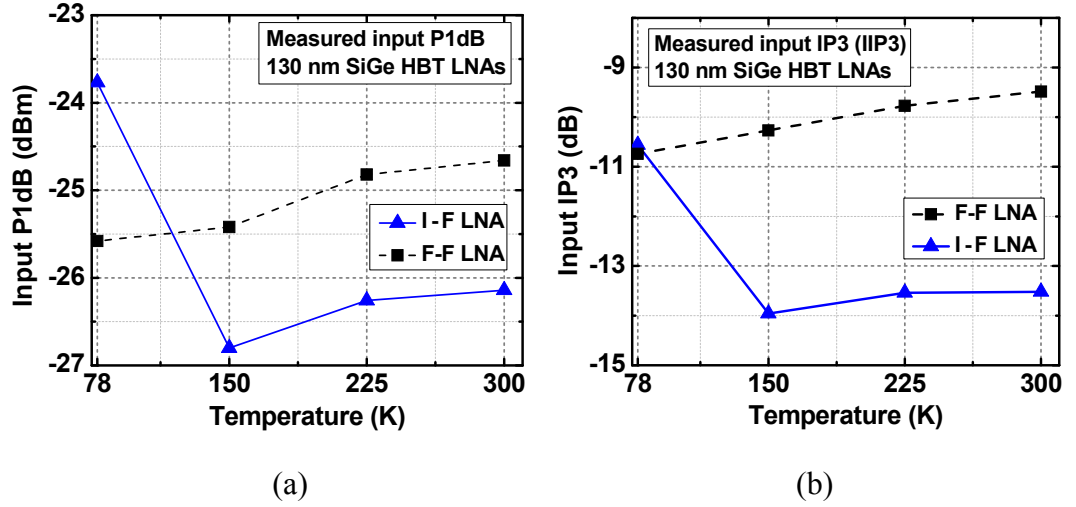


Figure 4.5 - (a) Measured input 1-dB compression point (P1dB) for both the I-F and the F-F cascode LNAs versus temperature. (b) Measured input third-order intercept point (IP3) of both the LNAs versus temperature.

The measured RF linearity of the LNAs is presented in Figure 4.5. In Figure 4.5 (a), the measured input 1-dB compression point (P1dB) across temperature is shown. Except for 78 K, the I-F cascode LNA has lower input P1dB than the F-F cascode LNA. While the F-F cascode LNA exhibits the monotonic decrease in input P1dB due to gain increase, the I-F cascode LNA has the highest P1dB at 78 K, which is expected from the gain reduction at 78 K in Figure 4.3 (b). While the gain difference of the I-F cascode LNA at 300 K and 78 K is small, about 0.5 dB in Figure 4.3 (b), the input P1dB at 78 K is about 2.5 dB higher than the 300 K input P1dB. The measured input third-order intercept point (IP3) under a two-tone input condition is shown in Figure 4.5 (b). The overall trend of the input IP3 is similar to the input P1dB response in Figure 4.5 (a).

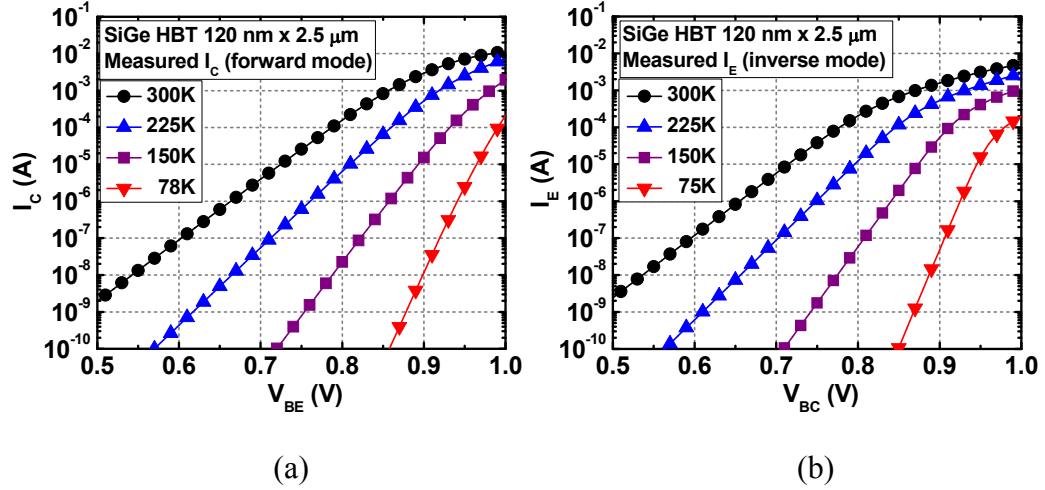


Figure 4.6 - Measured electrical collector current versus base voltage for different temperatures for (a) a forward-mode SiGe HBT and (b) an inverse-mode SiGe HBT.

Based on the characterization results over temperature in the previous section, the I-F cascode LNA provides acceptable RF performance as a cryogenic LNA for extreme environment applications. It exhibits enough gain, low noise figure, and good linearity at low temperatures down to 78 K. However, circuit designers and system architects should pay attention to a noticeable gain drop at 78 K in the initial design phase, since it may cause unexpected performance degradation or system malfunction for proper receiver operation. Because this gain decrease is observed only in the I-F cascode LNA compared to the conventional F-F cascode LNA, we need to investigate the behavior of inverse-mode SiGe HBTs over temperature.

One possible reason for the gain reduction of the I-F cascode LNA at 78 K is the disturbance from the proper bias point. The measured electrical collector current of both a forward-mode and an inverse-mode SiGe HBT is shown in Figure 4.6. From the comparison between Figure 4.6 (a) and (b), it is observed that overall electrical collector

current is similar for both operation modes at the same electrical base-emitter voltage. Noticeable difference between the two operation modes is that the high injection effect, which shows gradual slope in electrical collector current, occur at lower base voltage for the inverse-mode operation. Therefore, if both the forward-mode and the inverse-mode SiGe HBTs are biased at the same DC branch current, the latter is more likely to suffer from the Kirk effect. When the temperature goes down, the performance degradation can become more severe, since the current handling capability significantly reduces, pushing the device further into a high-injection condition for the inverse-mode. In the LNA measurement, each transistor is biased at 1mA for all temperatures. Under this operation condition, the inverse-mode SiGe HBT is quickly biased into a deep high-injection region at 78 K, which causes the reduction of f_T . Furthermore, as the requisite V_{EC} for providing the constant branch current increases at lower temperature due to the flatter slope, the resulting V_{CE} available for the common-emitter (Q_1 in Figure 4.1 (b)) becomes smaller under the fixed V_{CC} , biasing the Q_1 transistor in the deep saturation region. Therefore, the overall gain reduction is aggravated more than the F-F cascode LNA.

In order to mitigate performance degradation associated with inverse-mode SiGe HBTs, a few suggestions are followed. First, constant current biasing is not a preferred approach for wide range of operation temperature, since 1) the electrical collector current (or Gummel) varies significantly across temperature and 2) the inverse-mode SiGe HBTs easily suffer from high-injection effects. Thus, an adaptive bias scheme, which sets the optimal bias point by tracking the ambient temperature, should be considered in the circuit design [85], [86]. Second, the layout of the inverse-mode SiGe HBTs needs to be optimized for the best RF performance. For example, as described in [8], increasing the width of

physical emitter or decreasing the extrinsic collection region will help enhance the high frequency performance of the inverse-mode SiGe HBTs, compensating for the limited f_T at cryogenic temperatures.

4.4 Summary and Implications

The cryogenic characterization results of the inverse-mode-based SiGe HBT LNA is presented. In order to assess suitability for extreme-environment applications, we investigate the cryogenic operation of the single-event-hardened cascode LNA (termed I-F cascode LNA), in which an inverse-mode SiGe HBT is used in the place of a common-base stage. The I-F cascode LNA fabricated in a 130 nm SiGe BiCMOS platform exhibits acceptable RF performance for the cryogenic operation down to 78 K. A noticeable gain reduction is observed at 78 K, which can be attributed to non-optimal bias point for the cascode structure and limited RF performance of the inverse-mode SiGe HBTs. As a practical approach, two design techniques of adaptive biasing and layout optimization are suggested.

CHAPTER 5. WIDEBAND RF CIRCUIT DESIGN

5.1 Design of a Compact, Low-Loss, Wideband Attenuator

5.1.1 Introduction

Recently, many wideband high-performance transceiver (T/R) chipsets have been developed in silicon-germanium (SiGe) BiCMOS technology [88]. Since SiGe heterojunction bipolar transistors (HBTs) provide improved radio frequency (RF) performance parameters such as unity-gain frequency (f_T) and maximum oscillation frequency (f_{MAX}) vs. CMOS transistors at similar technology nodes, they are well-suited for wideband and high-frequency system applications [49]. In addition to these favorable RF parameters, small parasitic capacitance associated with SiGe HBTs further enables design of wideband RF circuits and T/R chipsets [89] because the smaller capacitance will increase the cut-off frequency (f_c) of artificial transmission lines, which have been often used in a distributed amplifier topology. In addition to the small-signal parameters, SiGe HBTs provide improved large-signal performance, including peak output power and 1 dB compression point [49]. Therefore, SiGe HBTs are good candidates for design and implementation of active circuits such as wideband amplifiers and multipliers.

While SiGe HBTs offer significant benefits to active circuits, some passive circuits still need to be designed in CMOS and can be naturally accomplished within a SiGe BiCMOS platform. In our simplified architecture of a 2-20 GHz single-channel wideband TTD-based T/R chipset (Fig. 1), a true-time delay (TTD) circuit and an attenuator require minimized insertion loss for their operation. Since CMOS devices provide low ON-state

resistance (R_{ON}) with zero power consumption compared to SiGe HBTs, which need DC current for biasing, these passive circuits are typically designed with CMOS. In addition, as RF nFETs in a typical BiCMOS platform exhibit moderate RF performance, they do not impose bandwidth limitations for the design of the wideband T/R chipset (Figure 5.1.1).

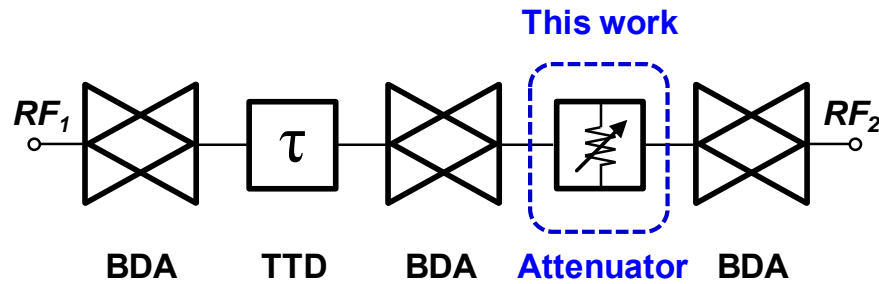


Figure 5.1.1 - System configuration of a 2-20 GHz SiGe BiCMOS single-channel wideband TTD-based T/R chipset. It includes bi-directional amplifiers (BDA), a true-time delay (TTD) circuit, and an attenuator.

With regard to attenuator design, attenuators are used in the control of side-lobes in antenna radiation patterns [39]. In order to provide controllability to such systems, attenuators should provide variable attenuation, which can be implemented with either analog or digital circuitry. The latter, digital control, is a more reliable and convenient method than the former, in the aspect of simplified system design. Among many performance parameters including insertion loss (IL), impedance matching, bandwidth, and attenuation range, small IL is critical for reducing the number of loss compensation amplifiers in the organization of multi-channel wideband T/R chipsets. Since additional

amplifiers are likely to increase system complexity, power consumption, and potential instability, attenuators should provide minimized IL.

Recent state-of-the-art digital-step attenuators (DSAs) have utilized T- or π -type attenuation cells and series/shunt switches for path selection control [39]-[41]. In [39], [40], switched T- and π -type attenuation cells were used for the attenuators. However, the loss associated with each series switch transistor amount to significant IL in the entire attenuators at high frequency. In [41], un-switched T-type and reduced T-type cells were combined with single-pole-double-throw (SPDT) and double-pole-double-throw (DPDT) switches. While the reduced T-type attenuation cell helped minimize the IL, the DPDT switches required more inductors for input/output and internal matching, increasing the overall chip size. In addition, DPDT-based topology requires an input signal to see one more series switch transistor than the number of T-type attenuation cells, inevitably further degrading IL.

In this chapter, we propose a wideband DSA with 6 bit digital attenuation control. It is based on the hybrid combinations of switched T-type attenuation cells for high attenuation cells (4, 8, and 16 dB) and reduced T-type cells [41] for low attenuation cells (0.5, 1, and 2 dB). The proposed DSA exhibits low IL across wide operational bandwidth (DC-20 GHz) and compact chip size compared to other state-of-the-art DSA designs.

5.1.2 Digital-Step Attenuator Design

One of the conventional attenuator topologies is a switched T-type attenuation cell, as shown in Figure 5.1.2 (a). In a switched T-type attenuator, two series resistors (R_1) and a shunt resistor (R_2) perform signal attenuation, while a series switch (M_1) and a shunt

switch (M_2) control the operation depending on the V_{ctrl} signal. Among two switch transistors (M_1 and M_2), the series switch M_1 determines the overall insertion loss (IL) which is a key performance parameter for an attenuator. Since M_1 will have finite R_{ON} , the size of M_1 should be large enough for minimizing the loss associated with R_{ON} . However, because the parasitic capacitance of M_1 inevitably increases with larger device size, the isolation performance of the M_1 switch becomes less effective in decoupling in/out and out/in ports from each other (Figure 5.1.2 (a)). Thus, one needs to find the optimum size for balancing IL and isolation.

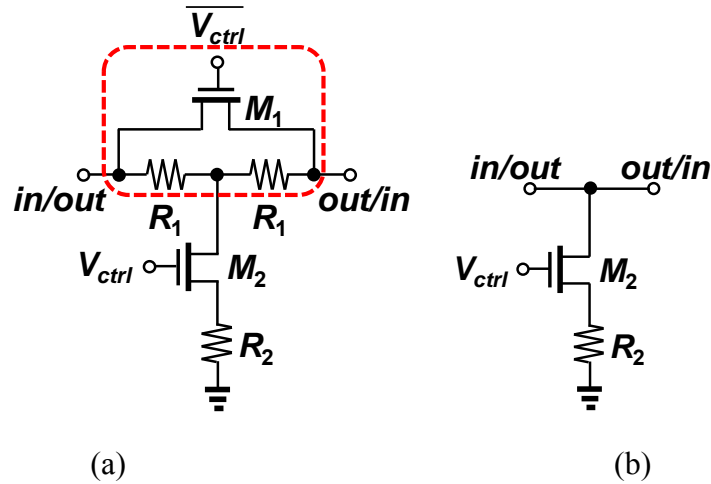


Figure 5.1. 2 - (a) Schematic of a conventional switched T-type attenuation cell (b) Schematic of a reduced T-type attenuation cell. The series switch transistor (M_1) and resistors (R_1) are removed for the minimization of insertion loss.

When the attenuator consists of multiple attenuation cells for multi-bit control, the accumulated IL of the entire circuit can be too large for proper system operation. As mentioned above, since the main loss occurs in the series transistors (M_1), reducing the

number of series switches is critical to obtain low IL of the attenuator. For lower-dB attenuation, such as 0.5 dB or 1 dB, the required value of R_1 becomes much smaller than the values of R_2 in conventional T-type cells. For example, the 0.5 dB and the 1 dB attenuation need R_1 of 1.4 and 2.9 Ω , respectively, whereas R_2 requires 868 and 433 Ω , respectively.

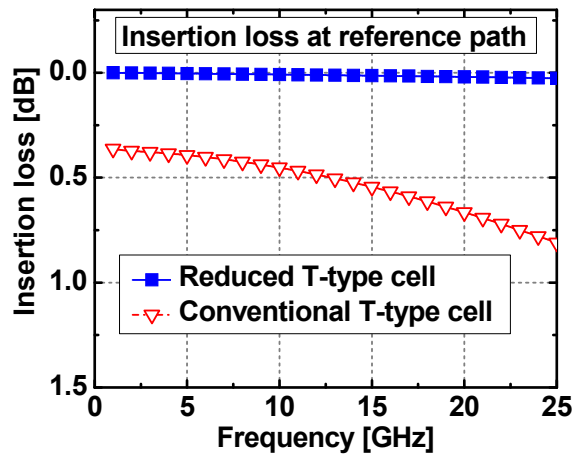


Figure 5.1.3 - Simulated insertion loss of a conventional cell and a reduced T-type cell for the reference path.

From a practical point of view, the relatively small resistors in low-attenuation cells can be simply removed from the schematic [41]. If two R_1 resistors are deleted from the T-type cell, the series switch M_1 can also be taken out without any loss of its function. The absence of the series switch will result in lower IL than the conventional T-type attenuation cell. The simulated IL of the reduced and the conventional T-type cells for the reference path are shown in Figure 5.1.3. While the conventional cell showed the minimum IL of 0.36 dB, the reduced cell exhibited almost negligible IL. The overall difference in IL

between conventional and reduced cells will be larger when multiple attenuation cells are cascaded for the implementation of a DSA. In addition, the IL of the conventional cell was more frequency-dependent than the reduced cell counterpart. This is attributed to the parasitic capacitance of the series switch transistor, which often requires the addition of inductors in order to resonate out the capacitance. However, the use of additional inductors inevitably increases design complexity and the total chip size. Therefore, the reduced T-type attenuation cells provide the benefits of minimized IL, mitigated frequency dependency, and smaller chip size, compare to the conventional approach.

In addition, the use of such small resistors in a schematic often causes issues in circuit layout design. Typically, obtaining such small resistances in an integrated circuit (IC) design environment is not a simple process. Small resistance can be obtained by connecting many short, wide resistors in parallel, resulting in larger circuit area as well as a complexity increase for accurate electromagnetic (EM) simulations.

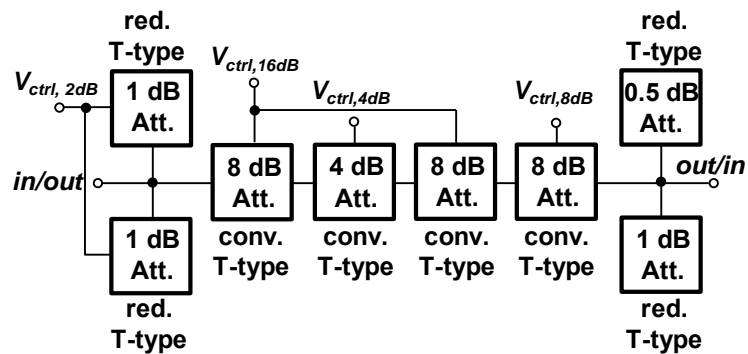


Figure 5.1.4 - Simplified schematic of the proposed wideband digital-step attenuator. Inductors need to be inserted between attenuation cells for better impedance matching. It has 6 digital bits to control attenuation. For 2 dB and 16 dB attenuation cells, two 1 dB cells and two 8 dB cells were used, respectively, for the implementation.

The full schematic of the proposed wideband low-loss digital-step attenuator is shown in Figure 5.1.4. It has 6 digital bit inputs which set independent control of binary-coded attenuation levels (0.5, 1, 2, 4, 8, and 16 dB). High attenuation cells including 4, 8, and 16 dB use the conventional switched T-type cells, while low attenuation cells (0.5, 1, and 2 dB) use the reduced T-type cells. The 16 dB cell consists of two 8 dB cells in order to minimize phase error. Similarly, the 2 dB cell is composed of two 1 dB cells for better impedance matching.

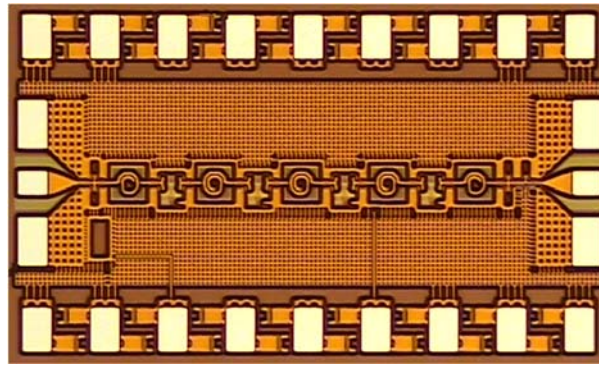


Figure 5.1.5 - Chip micrograph of the fabricated wideband digital-step attenuator. The active core size excluding measurement pads was 1.0 mm x 0.14 mm and the total chip size was 1.3 mm x 0.75 mm.

5.1.3 Experimental Results and Discussion

The proposed wideband digital-step attenuator was fabricated in Global Foundries 130 nm 8HP SiGe BiCMOS technology platform, which provided triple-well RF nFETs with an f_T of about 90 GHz. The proposed attenuator used coplanar waveguide lines with ground plane (CPWG) for signal lines. Lumped inductors were inserted between

attenuation cells for better input/output impedance matching, and all inductors and passive interconnection structures were simulated and optimized with an EM simulation tool (Sonnet) for accurate parasitic modeling and minimized amplitude/phase error. In addition, each series and shunt switch transistor employed a floating-body technique for minimizing signal leakage through substrate junction. Power supplies of 2.5 V and 1.2 V were used for N-well biasing and V_{ctrl} , respectively. A chip micrograph is shown in Figure 5.1.5. The core attenuator circuit area excluding measurement pads and non-active space was 0.14 mm^2 ($1.0 \text{ mm} \times 0.14 \text{ mm}$), while the total chip size was 0.98 mm^2 ($1.3 \text{ mm} \times 0.75 \text{ mm}$).

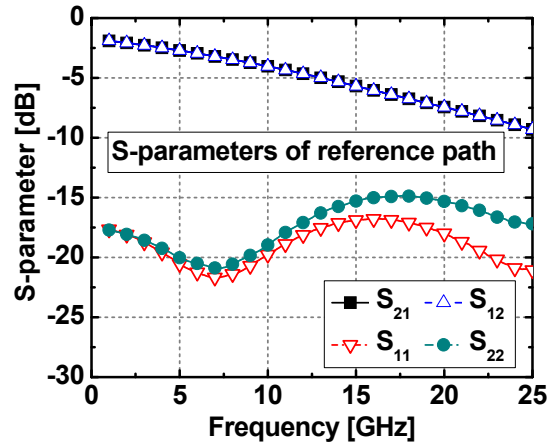
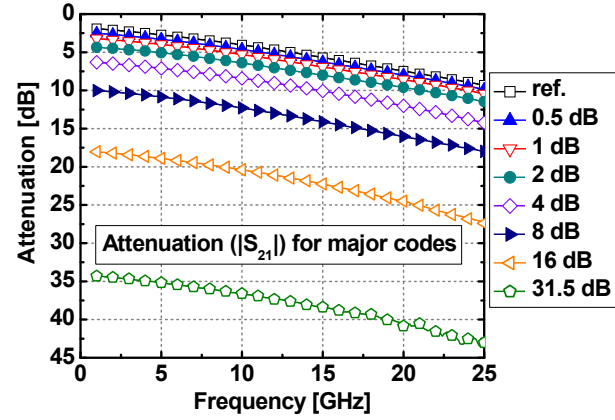


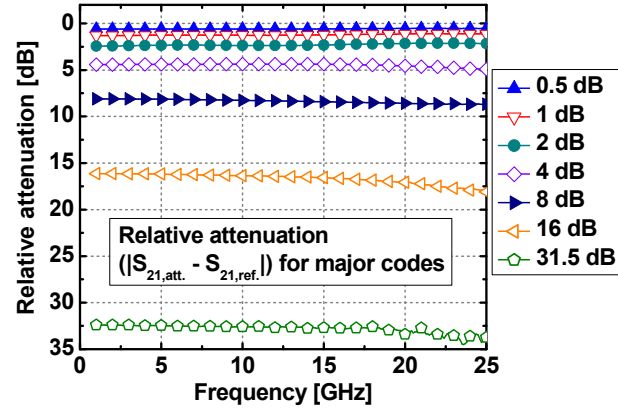
Figure 5.1.6 - Measured S-parameters of the proposed wideband digital-step attenuator for the reference path (without any attenuation).

The measured S-parameters of the proposed attenuator for the reference path (without any attenuation) are presented in Figure 5.1.6. Both of the input and the output matching showed good return loss below 15 dB up to 25 GHz. The IL was 1.9 dB at 1

GHz, 4.0 dB at 10 GHz, and 7.4 dB at 20 GHz. Both of the forward IL ($-S_{21}$) and the backward IL ($-S_{12}$) exhibited similar response over the entire frequency.



(a)



(b)

Figure 5.1.7 - (a) Measured attenuation versus frequency for major attenuation codes. (b) Measured relative attenuation against the reference path versus frequency.

The measured S-parameters (S_{21}) over frequency for major attenuation codes are shown in Figure 5.1.7 (a). It includes the reference path, 0.5, 1, 2, 4, 8, 16, and 31.5 dB attenuation cases. For the maximum attenuation (31.5 dB), all digital control bits were

turned on. Since the maximum attenuated S_{21} parameters were close to the minimum sensitivity level of the vector network analyzer (VNA) equipment, the measured S-parameters showed some measurement noise especially at high frequency above 18 GHz. The relative attenuation against the reference path is presented in Figure 5.1.7 (b). For low attenuation bits (0.5, 1, and 2 dB cases) where the reduced T-type cells were used, the relative difference in attenuation was fairly constant over the entire frequency. In contrast, the higher attenuation bits (4, 8, 16, and 31.5 dB cases) started to exhibit degradation at high frequency. This degradation is attributed to the parasitic capacitance associated with the series switches in the conventional T-type attenuation cells.

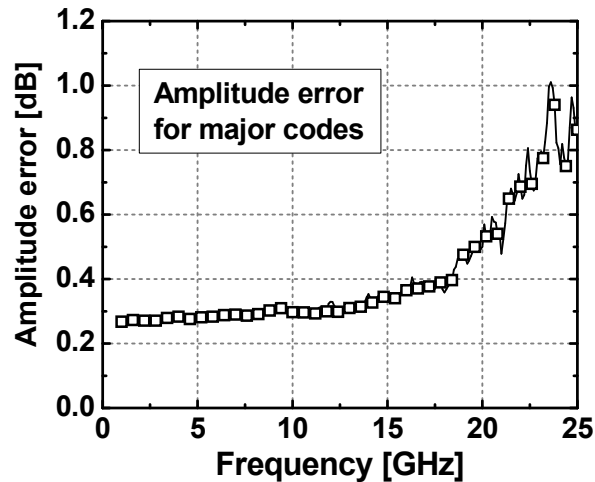


Figure 5.1.8 - Measured amplitude error versus frequency for major attenuation codes. For the operation up to 20 GHz, the maximum amplitude error was 0.5 dB.

The measured amplitude error versus frequency for major codes is shown in Figure 5.1.8. As frequency increases, the amplitude error almost monotonically increases (from 0.25 dB at 1 GHz to 0.5 dB at 20 GHz). The contribution of higher attenuation bits becomes

dominant at high frequency as expected from Figure 5.1.7 (b). Since the peak amplitude error is as large as the least-significant bit (LSB) of the proposed attenuator, further design optimization for high frequency operation is necessary for our 2-20 GHz wideband system in Figure 5.1.1.

Table 5.1.1 - Performance Comparison with State-of-the-Art Attenuators

Reference	[90]	[91]	[92]	[40]	[41]	This work
Process	GaAs FET	0.18 μm GaAs PHEMT	InGaAs pin diode	0.18 μm bulk CMOS	0.18 μm SOI CMOS	0.13 μm SiGe BiCMOS
Topology	Distributed T-type	N/A	π -type with pin diode	Switched T-/ π -type	DPDT/T-type SPST/red. T-type	Switched and reduced T-type
Bandwidth [GHz]	DC-20	1-15	7-40	DC-14	DC-20	DC-20
Attenuation range [dB]	22.5 (4 bit) (LSB=1.5 dB)	31.5 (6 bit) (LSB=0.5 dB)	31 (5 bit) (LSB=1 dB)	31.5 (6 bit) (LSB=0.5 dB)	31 (5 bit) (LSB=1 dB)	31.5 (6 bit) (LSB=0.5 dB)
Insertion loss [dB]	3.1-4.8	3.0-6.2	<11.5	3.7-10	3.1-7.6	1.9-7.4
Return loss [dB]	>13	>13	>8.0	>9	>12	>15
RMS amplitude error [dB]	0.5	0.25 @ 10 GHz	2.3	0.5	0.5	0.5
RMS phase error [°]	N/A	5 @ 10 GHz	N/A	4.2	2.5	10
Chip area [mm ²]	4.2 (2.6 x 1.6)	3.1 (2.6 x 1.2)	1.3 (1.6 x 0.8)	0.5 (1.25 x 0.4)*	0.63 (0.93 x 0.68)	0.98 (1.3 x 0.75) 0.14 (1 x 0.14)*

* Core circuit area without pads and non-active space.

The performance of the proposed wideband DSA is summarized in Table 5.1.1. The proposed DSA exhibits the lowest IL among the state-of-the-art attenuators in silicon platforms and the overall IL result is comparable to the attenuators in III-V technologies. In addition, the proposed DSA provides good impedance matching and low amplitude error

for wideband operation. It also occupies the smallest core chip area compared to other published designs.

5.1.4 Summary

In this section, a wideband digital-step attenuator for compact size and low insertion loss (IL) was implemented in SiGe BiCMOS technology. The proposed attenuator is based on the combination of conventional switched T-type cells and reduced T-type cells. By using the reduced T-type cells for low attenuation bits, the associated series switch transistors are removed, while impedance-matching performance is not degraded. As a result, the proposed attenuator achieves a minimized IL with good matching characteristics. In addition, by reducing the number of inductors in the schematic, the circuit exhibits compact chip size.

5.2 Design of a Bi-Directional Active Wideband Power Divider/Combiner

5.2.1 Introduction

Power dividers and combiners are key elements for realizing various radio frequency (RF) or millimeter-wave applications [93]-[96]. For multi-channel or phased-array systems such as imagers, radars, or communications applications, power dividers distribute generated source signals to each channel (or antenna) for beam forming or modulation, while power combiners add up incoming signals for subsequent data processing. In order to meet recent high-level system integration demands, designers need to build multifunction chipsets that support wide operational bandwidth with a compact, simple system architecture. A conceptual example of such a system is shown in Figure 5.2.1. The system consists of front-end modules, true time delay circuits, attenuators, and power dividers/combiners for implementing a multichannel configuration, wide bandwidth, and bi-directional operation. In this system, the power dividers and combiners should satisfy the same requirements for the system functionality.

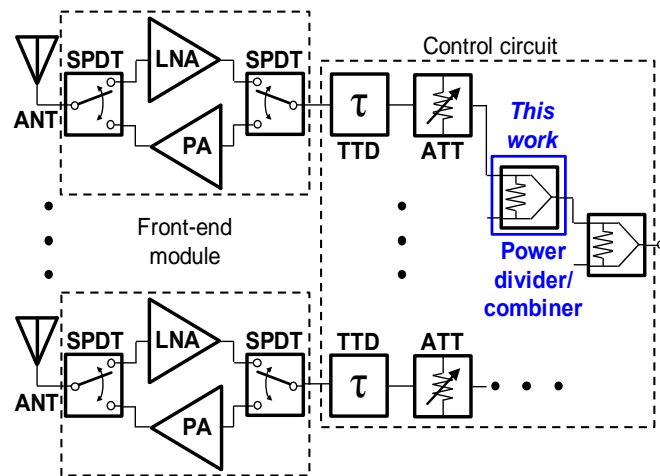


Figure 5.2.1 - System configuration of a multi-channel wideband phased-array transceiver chipset.

There have been a number of approaches for designing power dividers and combiners in the literature. One of the conventional designs is a passive-type power divider (or a combiner) such as the Wilkinson divider [30] and the Gysel divider [97]. As passive-type circuits, the power dividers and combiners support bi-directional operation, have zero power consumption, and exhibit high linearity. In addition, they are unconditionally stable with low noise figure (3 dB in an ideal case). However, they have the disadvantages of insertion loss, limited bandwidth, and large size. As a result of the parasitics associated the passive structures, the circuits inevitably suffer from loss of signal power. Moreover, the two-way power dividing operation exhibits 3-dB attenuation at each output. In a typical multichannel system, which requires multistage power dividing and combining [98], [99], the accumulated insertion loss may become significant, requiring additional gain amplifiers. However, the use of many gain amplifiers significantly increases system complexity and chip size. The other drawback of passive-type power divider and combiner circuits is their limited bandwidth. Because they utilize quarter-wave length transmission lines centered at a fixed center frequency or narrow-banded lumped inductors [100], a single-stage passive divider cannot support wide bandwidth. While a multi-section power divider can provide broadband response, it exhibits an increase in loss and chip size as a tradeoff [98], [99]. In addition, the large size associated with quarter-wave lines prohibits the use of the passive-type dividers in an integrated-circuit design environment, especially for low frequency applications [101].

Active-type power dividers and combiners, which use active gain stages for signal amplification, have been suggested as an alternative approach for passive-type circuits [31]-[38]. While active-type power dividers and combiners can compensate for the

insertion loss associated with passive circuits, they need to address additional issues such as stability, linearity, and power consumption in the initial design phase. Although in the literature various active power dividers and combiners have been proposed, most of the state-of-the-art designs have one of the following limitations. First, they support only uni-directional operation, requiring separate dividers and combiners for each transmitter and receiver [31], [33], [34], [36]-[38]. As a result, the overall system becomes larger in chip area and more complex in its configuration. Second, since they are based on III-V technologies [31]-[33], [35], [37], they are difficult to integrate with digital control blocks or other silicon-based logic circuitry, often leading to an increase in system development cost. Third, their operational bandwidth is narrow [34]-[36], which is not suitable for wideband applications.

In order to overcome the limitations associated with the previous designs, we propose a new wideband active power divider/combiner circuit [102]. Based on a bi-directional distributed-amplifier topology [103], the proposed circuit covers a wide range of frequencies from 2 to 22 GHz, which includes the entire S-, C-, X-, and Ku-bands. In addition, since the proposed divider/combiner circuit is implemented in a silicon-germanium (SiGe) BiCMOS technology platform, it provides seamless integration with CMOS digital circuits, all on a single chip. Depending on the control input, the circuit selectively operates in the divider or the combiner modes, enabling the design of bi-directional transceivers. Section 5.2.2 describes the design and the optimization of the wideband active power divider/combiner. In Section 5.2.3, the measured results are presented, followed by discussion. Section 5.2.4 will summarize the chapter.

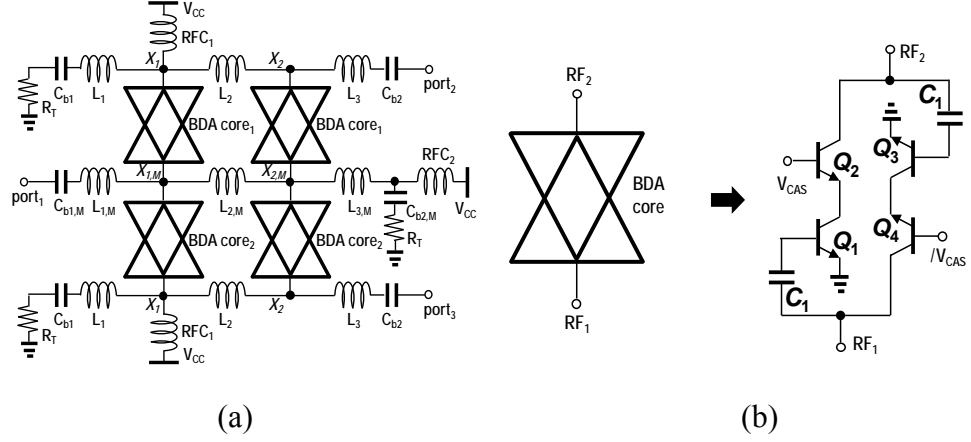


Figure 5.2.2 - (a) Full schematic of the proposed active power divider/combiner circuits (after [102]). (b) Schematic of the bi-directional amplifier (BDA) core.

5.2.2 Design of Active Power Divider/Combiner

The schematic of the proposed wideband active power divider/combiner circuit is shown in Figure 5.2.2 (a). The circuit is based on a two-stage distributed-amplifier topology with artificial transmission lines utilizing lumped inductors and parasitic capacitances associated with transistors [103]. The port₁ line is composed of L_{1,M}, L_{2,M}, and L_{3,M} and the capacitance at X_{1,M} and X_{2,M}, while the port₂ or the port₃ lines consist of L₁, L₂, and L₃ and the capacitance at X₁ and X₂. For the signal amplification under both the divider and the combiner modes, the proposed circuit includes four bi-directional amplifier (BDA) cores. In each artificial transmission line, a termination resistor (R_T) is added at the end of the line for wideband matching. Since the transmission lines have a characteristic impedance of 50 Ω, the termination resistors ideally have the same resistance. In addition, the proposed circuit includes integrated RF choke (RFCs) inductors (RFC₁ and RFC₂), which provide RF-open and DC-biasing paths from power supply (V_{CC}). DC-blocking capacitors (C_{b1}, C_{b2}, C_{b1,M}, and C_{b2,M}) are placed to present AC-short paths to RF signals,

preventing DC flow. The transistor-level schematic of the BDA core is shown in Figure 5.2.2 (b) without biasing circuitry. The BDA core has two cascode branches in the opposite directions such that the base terminal of Q_1 and the collector terminal of Q_4 are connected via C_1 and the same for Q_3 and Q_2 [103]. By applying high or low voltage to V_{CAS} , users can control the direction of the signal flow which determines the operation mode between a power divider and a power combiner.

The number of stages in a distributed amplifier (DA) can be determined based on the requirements of the system. In general, the gain and the output power of a DA will increase with additional gain stages. However, even with the infinite number of stages, there is an upper boundary for the maximum gain due to the loss associated with the input and the output transmission lines [104]. In addition, the bandwidth of a DA will increase with more gain stages, since the cut-off frequency (ω_C) of the input and the output transmission lines will increase with smaller ($L_{unit}/2$) and C_{unit} for a unit segment.

$$\omega_C = \sqrt{\frac{1}{L_{unit} \cdot C_{unit}}} \quad (1)$$

The trade-off of additional stages includes a larger chip area and more DC power consumption. In the proposed power divider/combiner circuit, the requirement of > 5 dB gain and > 0 dBm output power leads to a two-stage distributed-amplifier topology, which also satisfies the 2-20 GHz bandwidth specification for the system.

The small-signal equivalent circuit for each operation mode is shown in Figure 5.2.3. In Figure 5.2.3 (a), V_{CAS} is set high for the power divider mode and the corresponding signal flow is denoted with arrows. With the amplification from the BDA cores, the loss

associated with ideal power division (3 dB) and other parasitics can be compensated for the subsequent signal processing. The injected signal at port₁ drives four BDA cores and the amplified signals flow out of port₂ and port₃ with equal amplitude and phase. The reverse signal flow from port₂ to port₁ (or from port₂ to port₃) is significantly suppressed since 1) the Q₃-Q₄ branch current is in an OFF-state and 2) the Q₁-Q₂ branches have good reverse isolation associated with the cascode configuration [81]. In Figure 5.2.3 (b), the small-signal equivalent circuit for the power combiner mode is depicted. Because V_{CAS} is high, the signals injected from both port₂ and port₃ are amplified and combined at port₁.

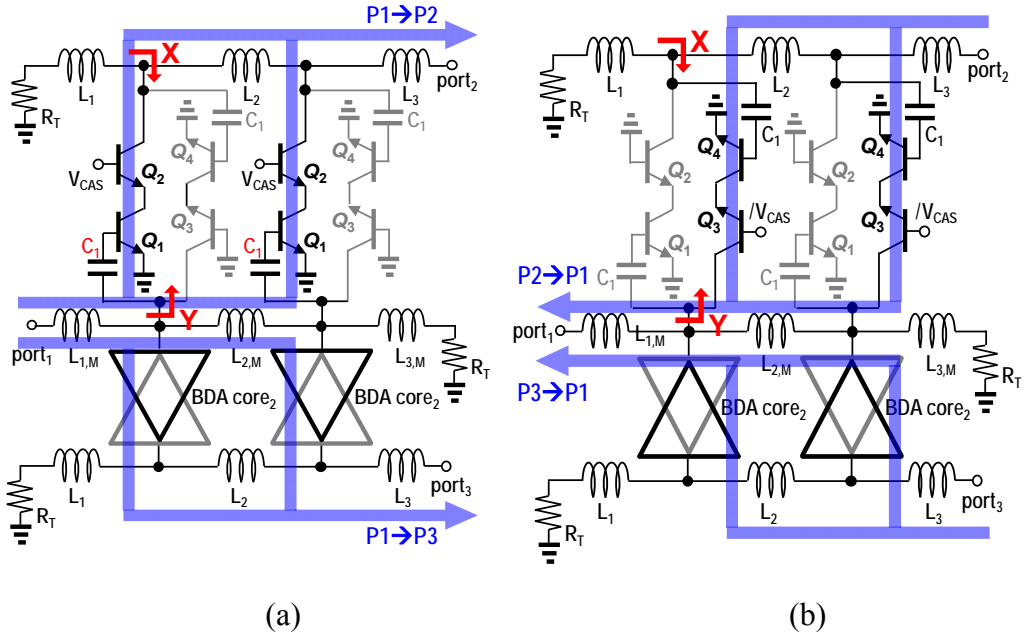


Figure 5.2.3 - Simplified small-signal equivalent schematic for (a) the divider mode and (b) the combiner mode.

For achieving wide operational bandwidth, the optimal design of artificial transmission lines (TLs) should be taken into account [105]. The characteristic impedance

(Z_0) of both the port_{2,3} and the port₁ TLs is obtained the following equations and it should be matched to 50 Ω .

$$Z_0 = \sqrt{\frac{2L_1}{C_{\text{total},X}}}, \text{ for the port}_{2,3} \text{ TLs} \quad (2)$$

$$Z_0 = \sqrt{\frac{2L_{1,M}}{2 \cdot C_{\text{total},Y}}}, \text{ for the port}_1 \text{ TL} \quad (3)$$

In (2)-(3), $C_{\text{total},X}$ and $C_{\text{total},Y}$ are the X and the Y node capacitance looking into the BDA cell, respectively. With regard to bandwidth, the port₁ line, which is composed of $L_{1,M}$, $L_{2,M}$, and $L_{3,M}$ (in Figure 5.2.3 (a)), is more band-limiting than the port₂ or the port₃ lines, since the shunt capacitance along the port₁ line is ideally twice larger than the port₂ or the port₃ lines. However, in order to maintain the fixed characteristic impedance Z_0 , larger shunt capacitance requires larger inductors, which in turn, limit the cut-off frequency of the transmission lines [105]. In addition, the phase propagation of each TL should be close to each other in order to maximize the distributed-amplifier performance. If the length of each section is much smaller than the wavelength, the phase shift (θ) associated with each section is expressed as follows.

$$\theta = 2\omega\sqrt{2 \cdot L_1 \cdot C_{\text{total},X}}, \text{ for the port}_{2,3} \text{ TLs} \quad (4)$$

$$\theta = 2\omega\sqrt{2 \cdot L_{1,M} \cdot C_{\text{total},Y}}, \text{ for the port}_1 \text{ TL} \quad (5)$$

The size of the devices in the DA unit should be carefully chosen. For wideband operation, it is important to maintain the same capacitance associated at both terminals in

a BDA cell. When the circuit is in the divider mode (Figure 5.2.3 (a)), the total capacitance at node X and Y looking into the BDA is derived as follows.

$$C_{\text{total},X,\text{div}} = C_{Q2,\text{col},\text{div}} + C_1//C_{Q4,\text{base},\text{div}} \quad (6)$$

$$C_{\text{total},Y,\text{div}} = C_{Q3,\text{col},\text{div}} + C_1//C_{Q1,\text{base},\text{div}} \quad (7)$$

In (6)-(7), $C_{Qx,\text{terminal},\text{operation}}$ denotes the capacitance looking into the Q_x device for the specific operation. Similarly, the total capacitance at node X and Y looking into the BDA under the combiner mode is expressed as follows.

$$C_{\text{total},X,\text{comb}} = C_{Q2,\text{col},\text{comb}} + C_1//C_{Q4,\text{base},\text{comb}} \quad (8)$$

$$C_{\text{total},Y,\text{comb}} = C_{Q3,\text{col},\text{comb}} + C_1//C_{Q1,\text{base},\text{comb}} \quad (9)$$

With the assumption that the collector capacitance of Q_2 and Q_3 in both the divider and the combiner mode is similar, and that the base capacitance of Q_1 and Q_4 is close, Q_1 and Q_4 need to have the same size in order to maintain the same total capacitance at the nodes X and Y. In addition, for the balanced small-signal and large-signal performance, it is practical to use the same-size devices for both common-emitter and common-base stages [106], [107]. Therefore, all active devices in a BDA have the same size in the proposed circuit in order to maintain the same operational bandwidth for both operation modes. The actual device size should be selected based on the circuit specification. In general, the larger device will lead to higher gain and better linearity with limited bandwidth. For low noise figure, large low-current-biased transistors are typically used with a trade-off in power gain and linearity.

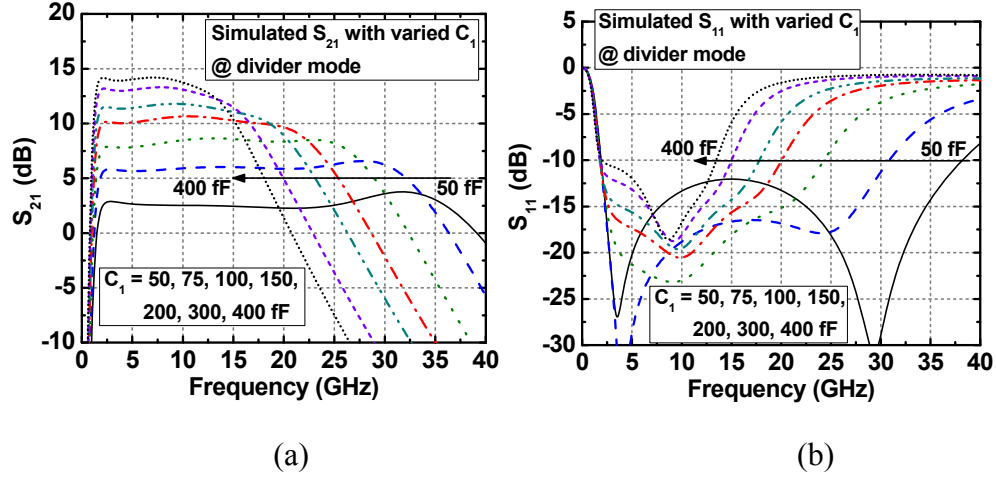


Figure 5.2.4 - (a) Simulated S_{11} of the proposed power divider/combiner circuit under the divider mode with varied C_1 (a) Simulated S_{21} with varied C_1 .

One of the design variables in this circuit is the C_1 capacitor shown in Figure 5.2.3 (a). It has two main purposes: one is to isolate the DC-biasing path from the AC-signal path and the other is to optimize the bandwidth of the proposed circuit. The effect of the C_1 capacitance is shown in Figure 5.2.4. Because C_1 is in series with the base-to-emitter capacitance of Q_1 , the total shunt capacitance (C_{total}) in the transmission line is reduced. In Figure 5.2.4 (a), the bandwidth of S_{11} decreases as C_1 increases (i.e., C_{total} increases). The bandwidth of 10-dB-return-loss reduces from 36 to 13 GHz. The simulated S_{21} with different C_1 is presented in Figure 5.2.4 (b). When C_1 becomes larger, the 3-dB bandwidth decreases accordingly. Therefore, the optimal C_1 capacitance should be selected for balanced gain and matching characteristics.

All transistors in the BDA cores (Figure 5.2.2 (b)) have the same emitter area of $0.12 \times 8.0 \mu\text{m}^2$ and the device-terminal layout of collector-base-emitter-base-collector (CBEBC), which improves high-frequency performance by reducing the base resistance [49]. The inductance of the RF chokes (RFC₁, RFC₂, and RFC₃) are 2.2 nH and the self-

resonant frequency is about 23 GHz. For more compact layout, the RF-choke inductors and the DC-blocking capacitors (C_{B1} and $C_{B2,M}$) can be removed if V_{CC} is directly supplied through the termination resistors. However, this approach will eventually lead to an increase in power consumption in order to maintain the same collector node voltages. In addition, L_1 , L_2 , and L_3 have an inductance of about 380, 530, and 300 pH, respectively, while $L_{1,M}$, $L_{2,M}$, and $L_{3,M}$ have inductances of 450, 530, and 350 pH, respectively. The termination resistors are $40\ \Omega$ for optimized and balanced performance. The layout of the circuit should be kept as symmetrical as possible for suppressing and minimizing amplitude or phase imbalance. The simulated mode-switching time between the divider and the combiner is about 600 ns.

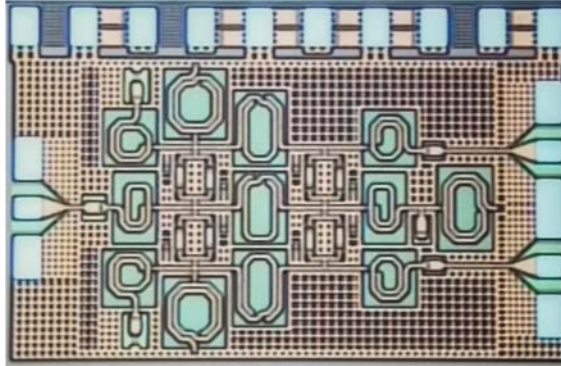


Figure 5.2.5 - Chip micrograph of the proposed wideband active bi-directional power divider/combiner circuit fabricated in a 130 nm SiGe BiCMOS platform. The size of the chip is $1.43 \times 0.92\text{ mm}^2$.

5.2.3 Measurement Results and Discussion

The proposed wideband active power divider/combiner circuit was fabricated in GlobalFoundries 130 nm SiGe BiCMOS platform (8HP), which features the unity-gain frequency (f_T) and the maximum-oscillation frequency (f_{MAX}) of 220 and 270 GHz,

respectively [45]. The chip micrograph is shown in Figure 5.2.5 and the chip size is 1.3 (1.43 x 0.92) mm². The circuit consumes a bias current of 40 mA from a 2.5 V power supply. For selecting an operation mode, the control input of 2.5 V is used. After the voltage drop across a biasing resistor, the base terminal of the ON-path cascode transistor is maintained at 2.1 V (with I_B of 23 μ A), while the voltage of the OFF-path cascode base is 0 V. For the four-port S-parameter characterization, a network analyzer (Agilent PNA E8364B) and a S-parameter test set (N4421A) were used, whereas analog signal generators (Agilent PSG E8257D) and a signal analyzer (Agilent PXA N9030A) were used for linearity measurements. For noise figure characterization, a noise source (Agilent N4002A) was connected to the signal analyzer.

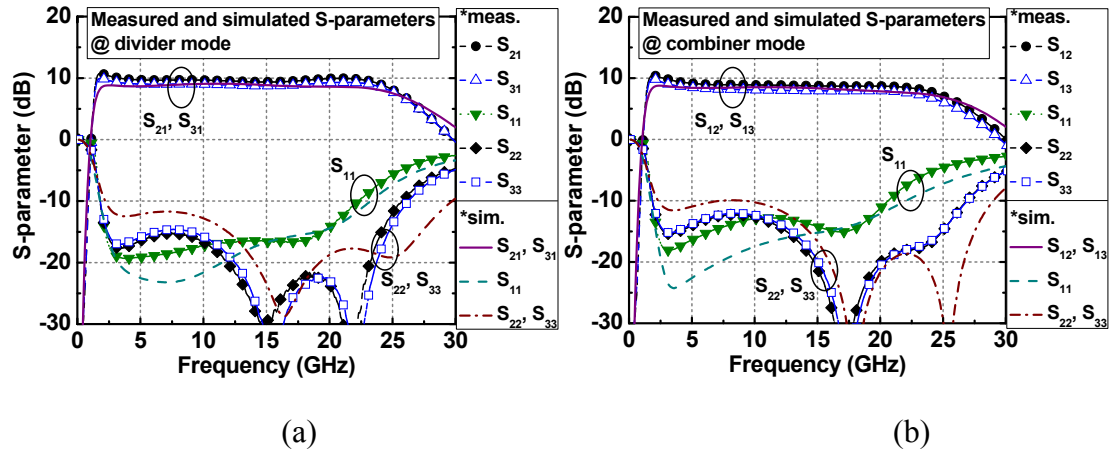
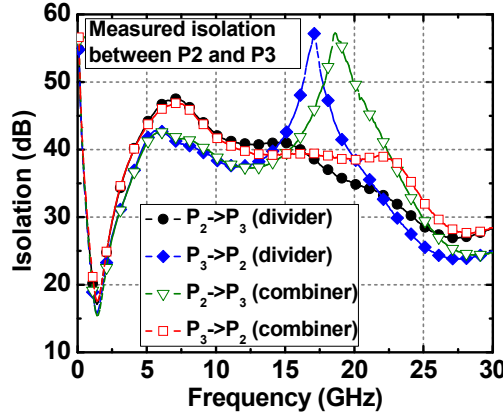
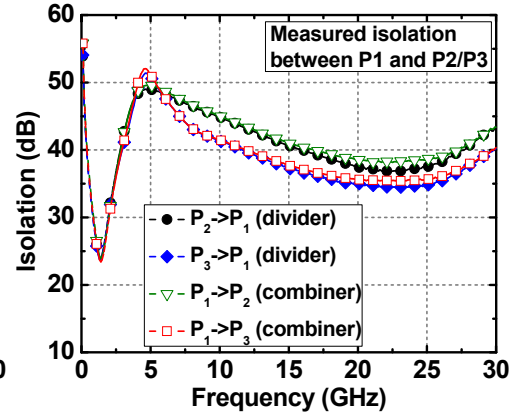


Figure 5.2.6 - Measured and simulated S-parameters of the proposed power divider/combiner circuit under (a) the divider operation and (b) the combiner operation.

The measured and the simulated S-parameters of the proposed power divider/combiner circuit are shown in Figure 5.2.6. The S-parameters were obtained from the three-port measurement set-up. The S-parameter response under the power divider mode is presented in Figure 5.2.6 (a). The 3-dB bandwidth of both the forward transmission gain (S_{21} and S_{31}) is 23.6 GHz from 1.4 to 25.0 GHz. In Figure 5.2.6 (a), S_{21} has two gain peaks of 10.8 and 10.0 dB at 2 and 22 GHz in the divider mode, respectively. On the other hand, in Figure 5.2.6 (b) only one peak of 10.4 dB is observed at 2 GHz in the combiner mode (S_{12}). This is mainly due to the asymmetries in the circuit layout and the mismatches in the branch biasing currents. In addition, the signal gain from port₁-to-port₂ is about 1.0 dB higher than the port₁-to-port₃ gain across the entire bandwidth for the divider mode. The slightly reduced gain of the combiner mode can be attributed to phase, cut-off frequency, and loss difference between the port₁ and the port₂ transmission lines. The 10-dB-return-loss bandwidths of S_{11} , S_{22} , and S_{33} are 20.0, 24.2, and 24.8 GHz, respectively. The S_{11} bandwidth is more limited than those of S_{22} and S_{33} , since the port₁ transmission line under sees larger capacitance than the port₂ or the port₃ lines, as explained in Section II. The measured and simulated S-parameters for the combiner mode is shown in Figure 5.2.6 (b). While the overall response is similar to the divider mode results, the gain (S_{12} or S_{13}) is lower than the divider mode and the 10-dB-return-loss bandwidth of S_{11} is slightly narrower.

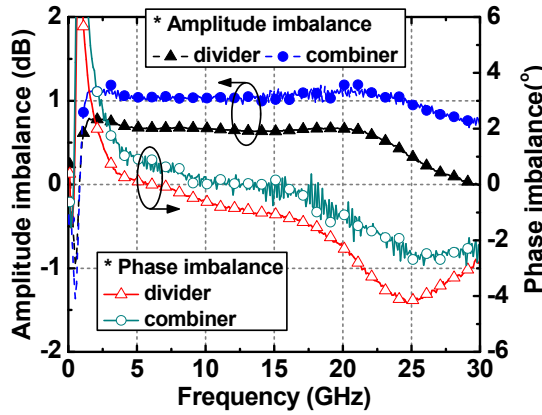


(a)

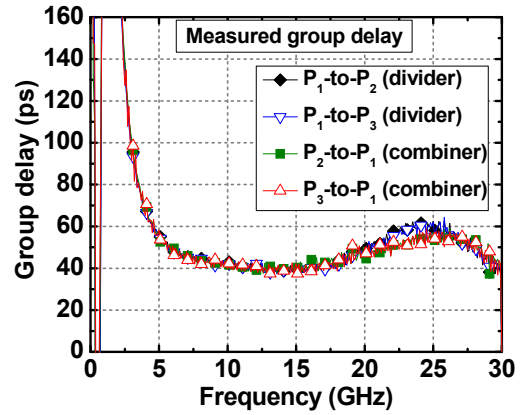


(b)

Figure 5.2.7 - (a) Measured isolation between port₂ and port₃ under both the divider and the combiner modes (b) Measured isolation between port₁ and port₂/port₃.



(a)



(b)

Figure 5.2.8 - (a) Measured amplitude and phase imbalance under both the operation modes (b) Measured group delay between port₁ and port₂ and between port₁ and port₃.

The measured isolation, imbalance, and group delay of the proposed power divider/combiner circuit are shown in Figure 5.2.7 and Figure 5.2.8. In Figure 5.2.7 (a), the minimum isolation between port₂ and port₃ for both the divider and combiner modes is

about 22 dB at 2 GHz. Below 12 GHz, the isolation response is similar for all cases, while two sharp peaks are observed around 17 GHz in some cases. In Figure 5.2.7 (b), the isolation between port₁ and port₂/port₃ is shown for both the divider and the combiner modes. The minimum isolation is 30 dB at 2 GHz. The amplitude and phase imbalance results are presented in Figure 5.2.8 (a). The amplitude imbalance is relatively flat within the entire in-band frequency. On the other hand, the phase imbalance of the divider and the combiner modes have different trends across frequency. The divider mode has monotonically decreasing phase imbalance from 2.1 to -3.3° with increasing frequency, while the combiner mode has a variation between 3.5 and -1.5°. The measured group delay results are shown in Figure 5.2.8 (b). In both the divider and the combiner modes, the overall group delay characteristics are similar for the paths between port₁ and port₂ or between port₁ and port₃. Except for the low frequency region below 5 GHz, the group delay varies between 40 and 50 ps. Due to the use of the integrated RF choke inductors instead of external RFCs or bias tees, the circuits exhibit large group delay for low frequencies [108].

The large-signal response under the divider mode is shown in Figure 5.2.9. In Figure 5.2.9 (a), the output power is measured at 10 GHz along the input power. As expected from the S-parameter measurements shown in Figure 5.2.6 (a), the port₁-to-port₂ gain is higher than the port₁-to-port₃ gain. From the large-signal gain response, the output and the input 1-dB compression points (OP1dB and IP1dB) are found to be 1.9 and -6.5 dBm for the port₁-to-port₂ path, respectively. In addition, the output power of the third-order harmonic frequency is measured with the two input tone frequencies of 20 MHz spacing. For the port₁-to-port₂ path, the output and the input third-order intercept points (OIP3 and IIP3) are

9.9 and 1.9 dBm, respectively. In Figure 5.2.9 (b), the OIP3 and the OP1dB are shown versus frequency. The OIP3 and the OP1dB of the port₁-to-port₂ path is about 2 dB higher than the port₁-to-port₃ results. The maximum OIP3 and OP1dB are 11.2 and 2.2 dBm, respectively.

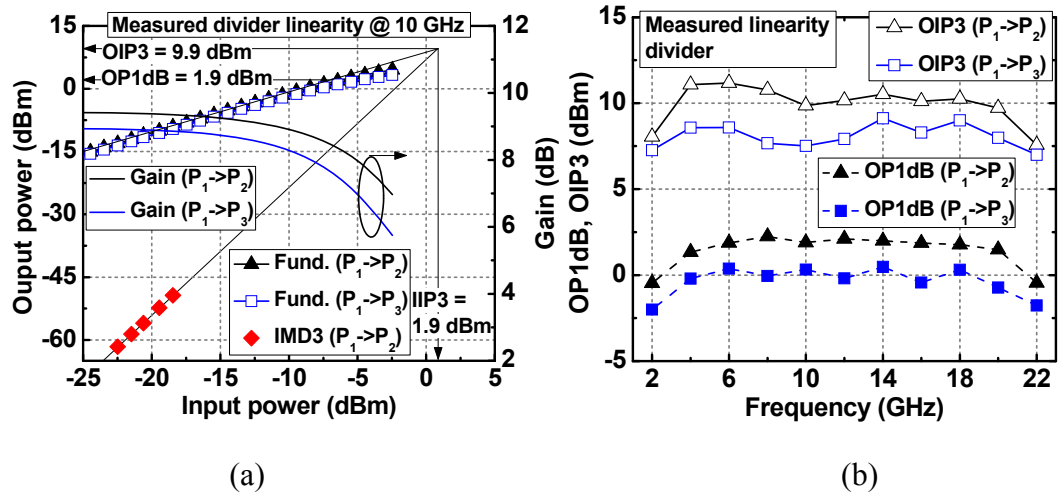
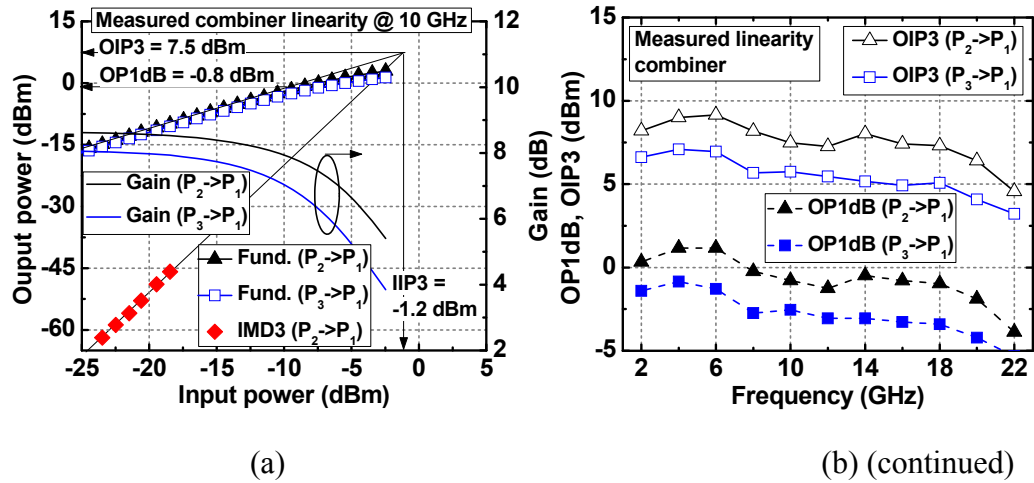
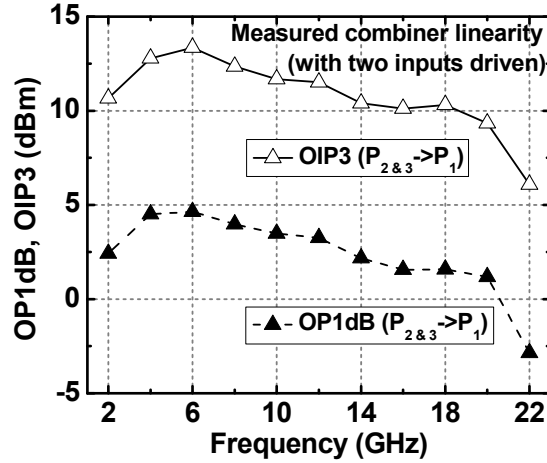


Figure 5.2.9 - (a) Large-signal response at 10 GHz. The fundamental output power and the corresponding power gain are shown versus the input power. In addition, the output power of the third-order harmonic is plotted. (b) Output P1dB and output third-order intercept point versus frequency under the divider modes.





(c)

Figure 5.2.10 - (a) Large-signal response at 10 GHz under the combiner mode (b) OP1dB and OIP3 versus frequency when only one port of the combiner inputs is driven (c) OP1dB and OIP3 versus frequency when two combiner ports are driven simultaneously.

The measured large-signal results under the combiner mode is shown in Figure 5.2.10. The power gain, OP1dB and OIP3 results are presented in Figure 5.2.10 (a). Compared with the divider mode results, the overall response is similar, but slightly lower. The OIP3 is 7.5 dBm and the corresponding IIP3 is -1.2 dBm. The measured OIP3 and OP1dB when only one of two input ports is driven by a signal generator are shown in Figure 5.2.10 (b). Across the entire frequency, the port₂-to-port₁ path has higher OIP3 and OP1dB than the port₃-to-port₁ path. The maximum OIP3 and OP1dB are 9.2 and 1.1 dBm, respectively. In Figure 5.2.10 (c), the OIP3 and the OP1dB response is shown when the two input ports of port₂ and port₃ are simultaneously driven by signal generators. This measurement condition represents a more practical operational condition for a power combiner, since in a multi-channel transceiver, it receives input power from each antenna and the combined power will be transferred to the subsequent signal processing chain, as

depicted in Fig. 1. While in this case, the OP1dB and OP1dB will ideally increase by 3 dB compared with the single-port-driven results (Figure 5.2.10 (b)), the actual measurement shows slight variation from a 3 dB increase due to the mismatch and the amplitude/phase imbalance between the port₂-to-port₁ and the port₃-to-port₁ paths. The maximum OIP3 and OP1dB under the two-port-driven condition are 12.8 and 4.5 dBm, respectively.

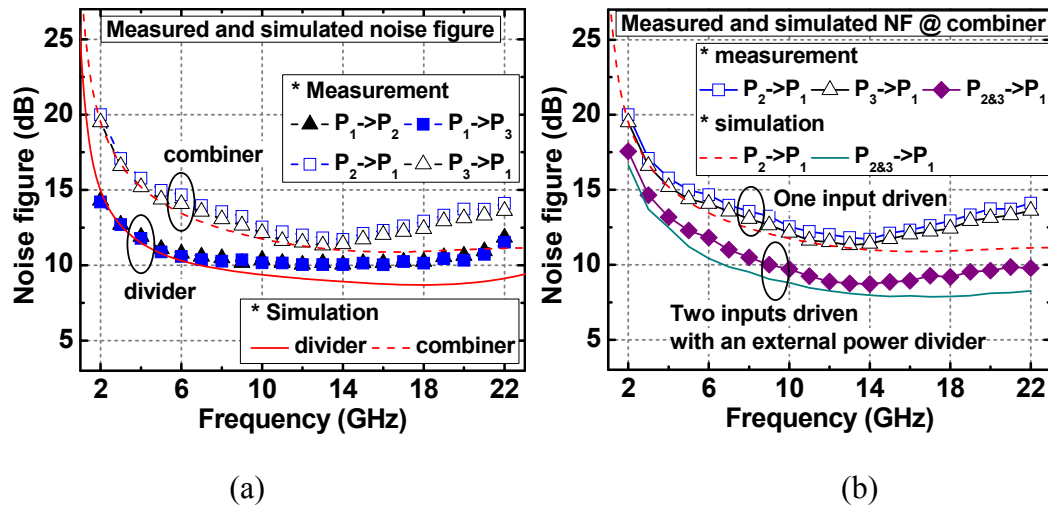


Figure 5.2.11 - (a) Measured and simulated noise figure under the divider mode (b) Measure and simulated noise figure under the combiner mode when only one input port is driven and when two ports are driven with an external power divider.

The measured noise figure (NF) versus frequency under both the divider and the combiner modes is presented in Figure 5.2.11. The NF response under the divider mode is flat from 8 to 20 GHz with the minimum NF of about 10 dB (Figure 5.2.11 (a)). Both the port₁-to-port₂ and the port₁-to-port₃ paths have similar NF characteristics. On the other hand, the combiner mode has slightly higher NF than the divider mode for the entire frequency band. The minimum NF is 11.3 dB at 13 GHz for the port₃-to-port₁ path. The NF of the port₂-to-port₁ path is about 0.5 dB higher than the port₃-to-port₁ path. The

measured and the simulated NF when the two combiner input ports are driven through an external power divider is shown in Figure 5.2.11 (b). Since each of the two signal paths provides power gain, the overall NF should decrease ideally by 3 dB, compared to the one-port-driven case where the other input is 50 Ω terminated [80]. However, the mismatch and the imbalance between the two gain paths results in some deviations. The minimum NF of 8.7 dB is observed at 13 GHz in the two-port-driven measurement.

Table 5.2.1 - Performance Comparison with the State-of-the-Art Active Power Dividers and Combiners

Reference	[33]	[33]	[37]	[36]	[35]	[32]	This work
Process technology	0.13 μm CMOS	0.13 μm CMOS	0.5 μm GaAs PHEMT	0.18 μm CMOS	GaAs FET	0.2 μm GaAs PHEMT	0.13 μm SiGe BiCMOS
Operation mode	divider only	combiner only	divider only	divider only	both	both	both
Circuit topology	artificial TL, DA, CS+delay cell	artificial TL, DA, CS+delay cell	cascaded amplifier, Darlington cell	artificial TL, DA, CS+cascode	artificial TL, DA, CS	microstrip, DA, CS	artificial TL, DA, cascode
Bandwidth (GHz)	1-10.6	1-10.6	DC-17.5	DC-20	0.8-2.15	2-18	2-22
Gain (div./comb.) (dB)	9.5	6	4.4	7.5	3/3	4.5/5.0	9.6/8.9
Isolation (div./comb.) (dB)	N.A.	N.A.	>23	>18	>22 / >24	15/12	>22 / >21
NF (div./comb.) (dB)	N.A.	5	N.A.	8	N.A.	N.A.	11/13
Amplitude/phase imbalance (dB/°)	N.A.	N.A.	0.1/2	0.9/0.9	N.A. / 3.5	N.A. / N.A.	0.8/3.5
OIP1dB (div./comb.) (dBm)	7.1	N.A.	-5	-10	N.A.	9	2/3
OIP3 (div./comb.) (dBm)	N.A.	N.A.	4.3	N.A.	N.A.	N.A.	11/12
P _{DC} (mW)	20.5	15.3	150	160	48	N.A.	100
Chip area (mm ²)	1.17	1.0	0.49	1.2	N.A.	3.0	1.3

***div.:** divider, **comb.:** combiner, **TL:** transmission line, **DA:** distributed amplifier, **CS:** common-source, **N.A.:** not available

The performance of the proposed power divider/combiner is summarized and compared with other recent state-of-the-art designs in Table 5.2.1. The fully-integrated proposed circuit simultaneously supports wide operational bandwidth (2-22 GHz), controllable bi-directional operation, and positive and flat in-band gain. In addition, by

using a silicon-compatible SiGe BiCMOS technology, it can be easily integrated with digital control circuits and other transceiver blocks. It also exhibits good isolation, impedance matching, amplitude/phase imbalance, and RF linearity (OP1dB and OIP3) in its bandwidth.

5.2.4 Summary

A wideband bi-directional active power divider/combiner circuit is proposed for multichannel broadband system applications. The circuit utilizes a two-stage distributed-amplifier topology with artificial transmission lines for wide operational bandwidth. In addition, it includes four bi-directional amplifier cores, which can selectively turn on or off one of two cascode branches for the given operation mode. The proposed power divider/combiner is implemented in a SiGe BiCMOS platform, providing the integration with digital control circuits on the same chip. The measurement results show wide bandwidth and high flat in-band gain with good port-to-port isolation, linearity, and impedance matching with under 100 mW DC power consumption.

CHAPTER 6. CONCLUSION

6.1 Summary of Contribution

This work investigates the design of RF building blocks for extreme-environment applications. In order to mitigate the single-event effects in RF circuits, inverse-mode SiGe HBTs have been applied to RF switches, low-noise amplifiers, and down-conversion mixers. With these SET-hardened circuits, front-end receivers have been designed and the transients are characterized in a functional level. In addition, the cryogenic operation of the inverse-mode SiGe-HBT LNA has been characterized and the impact of technology scaling on radiation-hardening techniques has been investigated. In terms of performance-driven design, wideband circuits have been proposed. The specific contributions include:

1. Design and the first demonstration of SiGe-HBT-based RF single-pole-single-throw switches for the mitigation of single-event transients. The optimal switch configuration has been investigated.
2. Application of inverse-mode SiGe HBTs in RF low-noise amplifiers and the first demonstration. The use of inverse-mode SiGe HBTs improves SEE tolerance with minimized performance degradation.
3. Investigation of the SEE-hardened down-conversion mixer with inverse-mode SiGe HBTs. This is the first demonstration of SiGe-HBT-based large-signal circuit using the inverse-mode operation. Device- and circuit-level analysis has been provided.

4. Design of SEE-hardened RF receivers with an inverse-mode-based switch, an LNA, and a mixer. Relative RF performance and SET sensitivity among different receivers has been studied.
5. Investigation of the impact of technology scaling on the applicable radiation-hardening techniques. With the advanced SiGe BiCMOS platform, the inverse-mode SiGe HBTs can be used for active gain stages with acceptable RF performance.
6. Cryogenic characterization of an inverse-mode SiGe-HBT-based LNA. Key parameters have been measured down to 78 K using liquid nitrogen.
7. Design of a wideband attenuator in SiGe BiCMOS technology. It exhibits the record insertion loss by minimizing the number of inductors and the series switch transistors.
8. Design of a wideband bi-directional active power divider/combiner circuit. This advances the stage-of-the-art by simultaneously providing wideband, positive gain, CMOS-compatible, and mode-selection features.

6.2 Future Work

There are several extensions of this research related to extreme-environment applications.

1. Complementary SiGe BiCMOS platforms offer performance-matched NPNs and PNPs. Design of PNP-based radiation-hardened RF circuit may be even more effective in SET mitigation.

2. Since advanced CMOS technology platforms show improved TID tolerance, the comparison of TID/SET sensitivity between CMOS and SiGe-HBT circuits becomes more meaningful.
3. Circuit-level radiation-hardening techniques including SET-filtering networks and dynamic SEE sensors.
4. Improving the performance of inverse-mode operation in a given technology can be a critical breakthrough for SET mitigation. Simple layout modification of SiGe HBTs will significantly enhance the RF circuit performance.
5. Cryogenic characterization of SET-hardened receivers and study of the device physics governing the inverse-mode operation. Accurate temperature-compensation circuitry is necessary.
6. Linearity improvement of wideband power divider/combiner. The use of hybrid cascode structure can extend the 1-dB compression point significantly.

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